Active Paralleling of High Power Voltage Source Inverters

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ABSTRACT

Power electronics are becoming established in ever broadening areas of industry. The transition from previous generation technology is driven by the opportunity for improvements in controllability, efficiency, and longevity. A wide variety of power semiconductors are available, however power handling capacity is still a significant limitation for many applications. An increase in the capacity of a single device is usually accompanied by a drop in switching frequency, and hence achievable system bandwidth. Increased capacity can be attained without this loss in bandwidth by using multiple lower power devices in parallel.

Products based on parallel device topologies are already present in the marketplace, however there are many associated complications. The nature of these complications depends on the control method and topology used, but no system combines high performance and high power with high reliability and easy maintainability. This research aims to identify and develop a method that would provide a system of voltage source inverters with a total capacity in excess of 10MVA, with effective control bandwidth comparable to a 100kVA system. Additionally, the method should be equally applicable at still higher power levels in the future with the anticipated development of higher capacity power semiconductors.

The primary goal when using paralleled devices is to achieve an even distribution of system load between them, as unbalanced load leads to poor system utilisation. Devices can be paralleled either passively, in which devices are controlled in common and characteristics inherent to the device are relied upon to balance load; or actively, in which devices are individually controlled and monitored to improve load balance. A key component of the thesis is the identification and analysis of the inadequacies inherent to passively paralleled systems. It is the limitations of passive paralleling that provide the motivation to develop an active parallel control mechanism.

Following the analysis, an active control algorithm is developed and implemented on a paralleled system. The proposed system topology consists of an array of medium power Voltage Source Inverter (VSI) modules operating in parallel. Each module is controlled semi-independently at a local level, with an inter-module communications network to enable active equalisation of module load, and redundant fault management. An innovative load equalisatiion algorithm is developed and proven, the key feature of which is this inclusion of a synthetic differential resistance between modules within the system.

The result is a modular expandable structure offering the potential for very high power capacity combined with quality of response usually only found in low power systems. The system as a whole is extremely reliable as any module can be isolated in the event of a fault without significantly affecting the remainder of the network.

Performance results from both simulation and experimentation on a two module small scale prototype are given. Using the developed topology and control method extremely accurate load balancing can be achieved without degradation of the response characteristics. The system is tested up to only $2.4kW$ in the course of this research, but the correlation with simulation is high and gives confidence that the developed mechanism will allow the $10MVA$ goal to be achieved.

Following the developmental stage of this research the technology has been applied to a com-

mercial system comprising parallel structures of up to 8 modules with a total power handling capacity of 1MVA with no deterioration in performance. 2MVA systems are deliverable with the current technology without any changes, and higher power levels are expected to be easily achieved.

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GLOSSARY OF TERMS

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
CAN	Controller Area Network
CCP	Common Connection Point
DC	Direct Current
DSP	Digital Signal Processor
GTO	Gate Turn-off Thyristor
HF	High Frequency
Hz	Hertz - unit of frequency
IGBT	Insulated Gate Bipolar Junction Transistor
LF	Low Frequency
LMS	Least Mean Squares
MCT	Metal Oxide Semiconductor Controlled Thyristor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
P	Real Power
P.U.	Per Unit
PWM	Pulse Width Modulation
VA	Volt-Ampere
VSI	Voltage Source Inverter
Q	Reactive Power
RMS	Root Mean Squared
SCR	Silicon Controller Rectifier
THD	Total Harmonic Distortion
t_s	Sample time
μ	micro $\Rightarrow 10^{-6}$
m	milli $\Rightarrow 10^{-3}$
k	kilo $\Rightarrow 10^{3}$
M	mega $\Rightarrow 10^{6}$
I	Current
R	Resistance
V	Voltage
X	Reactance
Z	Impedance

Chapter 1

INTRODUCTION

1.1 POWER SEMICONDUCTOR EVOLUTION AND THE CASE FOR PARALLELING

Power semiconductors appeared with the introduction of the thyristor in 1957. This was followed by the power bipolar junction transistor in the mid 1960's, which offered a significant advantage over the thyristor in that it could be actively turned off. This led to a revolution in power conversion technologies (motor drives, frequency converters, and DC power transfer networks to name but a few). The introduction of the power MOSFET in the late 1970's allowed vastly improved performance; they remain the standard for low power applications. Insulated Gate Bipolar Junction Transistors were developed in the 1980s, became widely available in the 1990's, and are currently the industry standard for most mid power applications. Each new technology developed bought with it significant performance advantages, however the refinement of the earlier devices has meant that a trade off must still be made in the design process depending primarily on the current, voltage, and switching frequency the device must work at, as illustrated in figure 1.1. At very high power levels, thyristor based devices such as the SCR, GTO, and MCT remain the only options. Further refinements are constantly being made to existing devices, and alternative technologies are being developed in an attempt to meet the demand for higher device performance, but at present no single device offers high power handling capacity combined with high practical switching frequency. The only way to acheive high power handling capacity at high switching frequency is to use multiple paralleled devices.

1.2 PARALLELING POWER SEMICONDUCTOR DEVICES

The development of topologies and control methodologies to allow paralleling of power semiconductors at either device or system levels is motivated by increasing demand from various areas

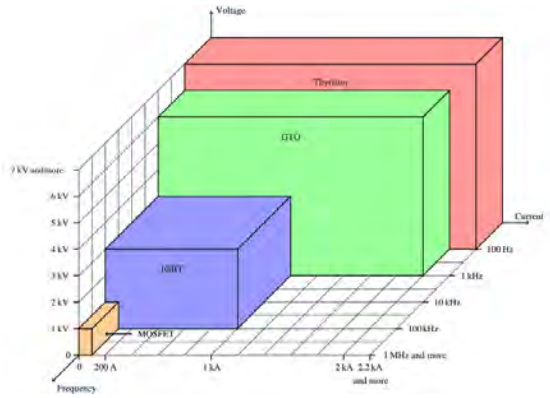


Figure 1.1 Power Semiconductor Device Operating Regions

of industry for high bandwidth, high capacity power converters.

Thyristor based devices can acheive the necessary power levels, however are unable to operate effectively at switching frequencies above $\sim 1kHz$, and as such they cause a bottleneck in the maximum achievable system bandwidth. In the case of a large transmission system the bandwidth requirement is not particularly high, as the fundamental system frequency is typically $50 - 60Hz$, and system transients are generally small in comparison to the system capacity. However frequency converters, power quality systems, motor drives etc can all reap significant benefits from switching frequencies in the $10kHz+$ range.

Referring back to figure 1.1, there is a clear relationship between switching frequency and power handling capacity for the various device families. Systems employing parallel device topologies are able to de-correlate those two parameters, granting access to a vastly increased performance envelope. Performance constraints associated with single high power device characteristics can be avoided. The most obvious benefit is an increased operating frequency at a given power level. This allows higher bandwidth control, and also the possibility of a smaller and lighter total system due to the smaller filter elements required at high frequencies.

In addition to an improved performance envelope, the use of multiple paralleled smaller devices/systems offers significant advantages over a monolithic power block.

- Reduced cost - The huge variation in the performance characteristics required of power electronic installations, whatever the application, can result in significant overheads due to time spent engineering a product to match a customers specific requirements. Resolving systems into smaller standardised modular blocks allows a tailored solution to be provided with minimal additional development time, and higher efficiency in production
- Flexible physical layout - The ability to create a high power system out of several smaller systems operating in unison allows adaptation to non-standard sizing requirements.
- Low downtime - The modular nature allows rapid replacement of faulty elements, avoiding expensive downtime.
- Improved quality - Modularity allows advanced test fixtures and highly skilled staff, as the one off costs in staff training and test fixture development are able to be spread over a larger number of items.
- Reduced stock holding requirement - On demand replacement part requirements can be met with a dramatically reduced number of in stock items.

To realise these benefits a new control method and system topology are required, the development of which is the goal of this research.

1.3 PARALLEL SYSTEM TOPOLOGY

When discussing the theory behind parallel module control it is valuable to have a clear definition of what constitutes a parallel system, the aim of the parallel control mechanism, and at what point the delineation between essentially monolithic system components and paralleled units is made.

A parallel system is a somewhat flexible notion, as the point at which the discretisation of modules occurs is heavily dependent on the control method in use. Consider that most individual power devices are themselves paralleled/seriesed arrays of smaller semiconductor devices. For example, a single power IGBT module composed of multiple IGBT dies is not considered a parallel system, as the component devices cannot be independently controlled. For all intents

and purposes, it is a single device. Likewise, the three IGBT half bridges of a 3 phase inverter are not considered paralleled, as their loads are not intrinsically matched. This thesis considers a paralleled system to be any system incorporating independently controllable power semiconductors all contributing to a common power path. This by no means dictates the point at which independent control does or does not occur; that distinction depends on the control system topology; the requirement is simply that it *could* occur.

The paralleling mechanism can be either active or passive. The distinction between active and passive paralleling in this thesis is made based on the presence of an element dedicated to load balancing in the control loop. Active paralleling requires that deliberate control action be taken to correct an imbalance in load. Examples of suitable actions are given in chapter three's control review.

Passively paralleled systems are those in which load balancing relies entirely on characteristics such as output filter impedance, device resistance, switching deadtime etc, as there is no *differential* (with regard to other modules/devices) change in control loop response or reference waveform as a result of unevenly distributed load. The relative simplicity is a strong argument in favour of passively paralleled systems, to be traded off against their potentially poorer performance. In chapter two, passively paralleled systems are further categorised as either hard or soft paralleled, the former consisting of directly connected modules while the latter involves the insertion of real impedance in modules outputs to mitigate transient imbalances.

This research focuses on the development of a control technique suitable for application to a paralleled network of Voltage Source Inverters (VSI's). While the techniques developed may be applicable to other similar systems, these alternate applications are not discussed.

1.4 PARALLEL SYSTEM GENERAL PERFORMANCE REQUIREMENTS

There are a variety of risks associated with parallel inverter operation. These vary depending on the topology and control method, but are never eliminated. At a fundamental level, most of the risks relate to an uneven distribution of losses among the semiconductors comprising the system. This leads to uneven thermal stress on devices, dramatically increasing the failure rate. Specific device parameters likely to cause imbalance are discussed in more detail in chapter 3. Losses within a device are proportional (if not directly proportional) to the power handled by that device. It follows that to equalise losses we must control power flow.

There are a number of system characteristics that must be preserved following the integration of a power flow control mechanism. Key among these are:

- Quality of response: Highly distributed systems such as those found on distributed generation grids share power by drooping (the droop process is explained in detail in the next chapter) some variable according to a common profile. Essentially the common output bus is used as a communications line. This is very efficient in terms of sensing and hardware requirements, but forces a severe compromise between bandwidth and accuracy of sharing, and quality of response. *The paralleling mechanism developed must preserve the output fidelity of the system*

- Noise Immunity: None of the systems reviewed used a digital communications network for paralleling. Analogue networks are not suitable for spatially distributed control in the high noise environment expected. *The developed mechanism must be tolerant of electrical noise to levels typically encountered in industrial environments*

- System Geometry: High power systems are often physically large, and spatially separated. The power flow control mechanism must support a distributed system architecture.

- Accurate Load Balancing: The aim of the control system is to balance load between the power devices according to some ideal distribution. To achieve the aims of this thesis the ideal distribution is power carried by each device proportional to the device rating. This ensures peak performance of the system, as no uneven device stressing will occur. The more accurate this distribution is the better, as any potential unbalance must be accounted for by derating the entire system. For example, to achieve a $1MW$ system consisting of 10 paralleled power modules with a worst case power imbalance of $\pm 10\%$ would require each module to be rated to $110kW$ to ensure the most heavily loaded unit does not exceed its rating. This is a significant waste of capacity, adding size and cost to the system. *The developed system must accurately balance load*

- Opportunity for expansion: Of the reviewed systems, those which display both good noise immunity and good quality of response are typically those based on a single processor controlling multiple power blocks. This is very nearly the opposite of the modular design that is desired, any expansion of the system will (assuming no change in the fundamental control approach) require a redesign of the existing control architecture and structure. The upper power module limit will likely be small, as it is restricted by the processing power and number of outputs present on the processor. These systems do not qualify as redundant, the processor being a single point of failure. *The developed system must be scalable*

1.5 AIM OF THIS RESEARCH

The focus of this research is the development of an effective method by which multiple independent VSI's can operate in parallel so as to form what is functionally a single VSI with a power rating equal to the sum of the parallel elements. The key concerns are applicability, reliability, and performance.

- Applicability: The resulting control algorithm and architecture should be suitable for paralleled systems in any configuration. Furthermore, it should be freely expandable to allow any number of modules to be present within the paralleled system, removing those constraints other than space requirements.

- Reliability: The system architecture and fault management processes should be designed such that the reliability increases with the number of modules in the system; continuing operation in the event of failure through redundancy, and the short time to repair offered by modularity outweighing the increased frequency of failure assured by increasing the number of units within a system. Essentially the availability must be at least equal to that of a monolithic system, where availability is expressed as:

$$Availability = \frac{MTBF}{MTBF + MTTR}$$

  where MTBF is Mean Time Between Failures, and MTTR is Mean Time To Repair.

- Performance: The performance of paralleled systems using the algorithm and architecture developed should be equal or better than the performance offered by a single module operating at the same power level.

1.5.1 Specific Performance Targets

- Output voltage distortion $< 1\%$.

- Module load imbalance $< 5\%$.
- Maximum system rating with $1MVA$ modules $> 10MVA$.

1.6 STRUCTURE OF THESIS

The remainder of this document is broken into 3 sections. Chapters 2 through 4 deal with the theory behind parallel system control and the development and theoretical performance analysis of parallel control algorithms. Chapters 5 and 6 cover the testing of the basic premise of the active paralleling mechanism, the hardware implementation of the system, and proof of performance on a prototype parallel system. Finally, chapters 7 and 8 return to theory to build on the knowledge gained from the experimental results and address the weaknesses identified. A new control algorithm that overcomes the weaknesses of the tested algorithm is developed and tested by simulation, and recommendations for future development are made.

Chapter 2

INVERTER PARALLELING TECHNIQUES

2.1 INTRODUCTION

The potential benefits of paralleled VSI systems have led to the investment of considerable development effort. Many of the early systems were passive in nature, relying entirely on incidental load balancing actions in combination with standard control methods, sometimes combined with output filter impedances, to keep the circulating current within reasonable limits. These systems are still widely employed due to their simplicity and robust nature, however their poor performance with respect to load sharing demands significant concessions are made during the design process.

Improvements in manufacturing methods has lead to a reduction in variances between components of the same model, which has important implications for passive paralleling. Additionally, the widespread availability of very powerful digital signal processors at low cost has opened the door to a new realm of feasible control methods, particularly with regard to distributed control topologies. The potential for improvement using active control methods has fostered a number of developments making extensive use of the proliferation of powerful microprocessors and robust high bandwidth communication networks.

There are two primary considerations in the search for an appropriate control mechanism, and in many cases they must be traded off against one another. The first is the fidelity of the system output with regard to the reference signal. If the control mechanism allows the paralleling of a large number of switching devices capable of operation in the 100kHz+ region, but in its action so heavily corrupts the output that the result is worse than could be achieved with higher power devices operating at sub kHz frequencies then it is of little use. Achievable parallel system output fidelity must be maintained close to that of an unparalleled system using similar devices if the parallel variant is to be attractive. The other consideration is the accuracy of load sharing. Any inaccuracy must be allowed for in system design as potential overhead in an individual module, that module and hence the whole system must be derated accordingly. Power semiconductors and their associated filters and heatsinks are expensive, hence a commercially attractive system will need to maintain the usable capacity as close to the installed capacity as possible.

This chapter begins with an explanation of some of the key principles influencing development of load sharing methods, then moves on to describe some of the methods previously developed. The field of general parallel power flow control is incredibly broad, ranging from the methods used for generators feeding national power grids, to sharing power between single semiconductor devices. However, the brief for this research is quite specific and as such this review deals only with methods that could be effectively applied to a centralised, medium power system of relatively high bandwidth.

2.2 KEY PRINCIPLES OF POWER ELECTRONIC LOAD SHARING

The aim of a parallel load sharing mechanism, whether passive or active, is to optimally distribute the system load between system power elements. All of the controllers examined retained a conventional voltage controller and, while the parallel mechanisms affected the output voltage, the primary regulation action remained the responsibility of the voltage controller. The sharing process should have minimal impact on the fidelity of the system output. The difference between load sharing and output regulation is easily understood as follows: Sharing the load can be seen as regulating the current that flows between modules within the system, while controlling the output voltage is a matter of controlling the net current flow through all the modules and into the system load.
Appendix A explains the theory of power flow between active sources. Ignoring for the moment the issue of minimising the distortion of the output, the problem of controlling current flow between modules, Δi simplifies to the following:

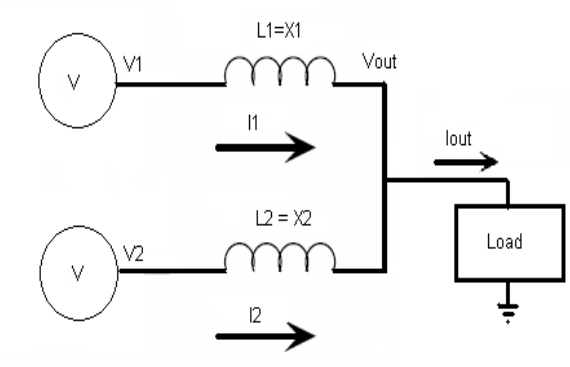


Figure 2.1 Current flow in a two element system

$$\Delta i = I_1 - I_2 = \frac{V_1 - V_{out}}{X_1} - \frac{V_2 - V_{out}}{X_2} \tag{2.1}$$

Assuming, for the sake of simplicity, that $X_1 = X_2 = X$ and there are no other modules on the system, the above becomes

$$I_1 - I_2 = \frac{V_1 - V_2}{X} \tag{2.2}$$

The differential current is purely a function of the differential voltage and the inter-module impedance. This is true regardless of the number of modules on the system, however in a multiple module system the imbalance with respect to a single other module is fairly irrelevant, the imbalance relative to the system average being a much more significant variable.

If we consider a system of equally rated modules, the objective of the paralleling mechanism is clearly to reduce the circulating current to zero. This can be achieved by reducing the differential voltage to zero, however the current also tends towards zero as the inter-module impedance tends towards infinity. Of the two methods, the minimisation of the differential voltage is preferable, as the addition of an output impedance, whether real or synthetic, invariably affects the output quality. Usually a combination of the two methods is used; the differential voltage is reduced as far as possible by accurate waveform generation and feedback, and a combination of real and synthetic impedance is used to minimise the current that flows due to the residual voltage difference.

It's also important that the impedance with respect to the common output buss is balanced between modules, as can be shown if we retract our assumption of $X_1 = X_2 = X$ in the above

case, instead use $2X_1 = X_2 = 2X$, and add an assumption that the differential voltage is zero; $V_1 = V_2$.

The differential current would now be

$$I_1 - I_2 = \frac{V_1 - V_{out}}{X} - \frac{V_1 - V_{out}}{2X} \Rightarrow I_1 - I_2 = \frac{V_1 - V_{out}}{2X} \tag{2.3}$$

This equates to inverter one carrying 1.5 times rated load, and inverter two carrying 0.5 times rated. Obviously such a large imbalance is unlikely in the case of a deliberately inserted impedance, however if parasitic impedances dominate it could easily occur in a large system with significant spatial separation.

The means by which specific control methods and topologies achieve the goal of load sharing, and the effectiveness with which they do so is the primary focus of this review; likewise the focus of this thesis is the development of a method which does it *better*.

2.3 PASSIVELY PARALLELED SYSTEM TOPOLOGIES

Load balancing relying entirely on characteristics such as output filter impedance, device resistance, switching deadtime etc is considered passive, as there is no *differential* (with regard to other modules) change in control loop response or reference waveform as a result of a load variation. A change in reference waveform resulting from the voltage regulation algorithm alone is not active load balancing, the key requirement is a differential change.

Attractions of passive paralleling are that it typically requires little additional technology compared to a stand alone system, as the paralleling action is dependent on characteristics that already exist in stand alone systems. The control action is the same by definition, which generally means only a small increase in computing power for even a large system. This relative simplicity could make passive paralleling an attractive option at first glance, but passively paralleled systems have significant disadvantages. The reliance on parasitics limits flexibility in design, and makes modular expandable systems very difficult to implement effectively. A common requirement is accurate matching of physical characteristics, which is difficult to achieve in large systems at commissioning, to say nothing of field replacement of failed modules.

Representatives of common passive paralleling methods are analysed briefly in this section, drawing primarily on previously published results.

2.3.1 Direct Connection

Direct connection is standard industry practice for large power devices, multiple semiconductor dies are connected in parallel and series within a single housing to increase the power rating of the device. The internal components are closely matched, and are not intended to be individually replaceable.

Direct connection in the context of paralleled power modules works on the same theory, but the challenges are significantly greater in consideration of the device tolerances available and end user requirements for serviceability etc.

Directly connected power modules share inputs, outputs, and all control signals, as shown in figure 2.2.

The primary benefit of this scheme is that as the paralleled power modules are treated as a single device it does not require any additional supporting infrastructure. Unfortunately, this strategy cannot be applied to arbitrarily large systems. While the detrimental effects of small device variations can be mitigated by careful matching when the number of devices in system is low, the variation between them, both initially and after the parameter drift which will inevitably

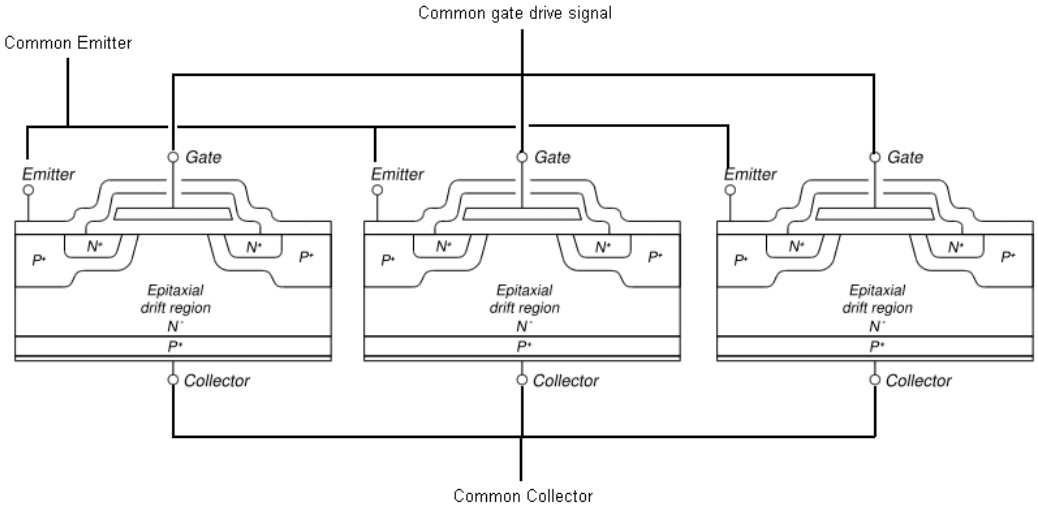


Figure 2.2 Direct Connection Topology Device Layout

occur over time, renders large systems unmanageable. This is quite aside from the logistics and cost of having large numbers of precisely matched devices. The parameters likely to result in assymetric load (hence device overloading), and system inefficiency are outlined below.

The primary complications identified with direct paralleling are as follow:

1. Variations in internal device parameters lead to unevenly distributed load and thermal losses. The most significant parameters are diode and transistor voltage drops and resistance.

2. Increasing the number of devices increases the possible switching time distribution, requiring increasingly large dead time to avoid a shoot-through situation.

3. The common gate signal will affect different switches at different rates. Any switch that turns on early or off late will carry a disproportionately large amount of current due to the common output connection.

4. Spatial separation will likely lead to different ambient temperatures for different devices on the same phase, which will further change the device characteristics, in addition to changing the effective device rating. Increased spatial separation will also required extremely high bandwidth control lines to avoid excessive propagation times.

5. Individual module failures are not fed back to the central controller, and there is no means of isolating a failed module, so not only will any failure will be catastrophic, but the failure frequency will increase with additional modules. Even if the module fails to a safe state the increased per unit current required of the remaining devices will almost certainly lead to a cascading failure of all modules.

6. Load balance in directly paralleled systems is very sensitive to the systems physical symmetry. Symmetrical layout is very difficult to achieve with the large structures necessary to handle high power.

Large directly connected systems are likely to be unreliable when operated at a significant percentage of their rated power. The catastrophic consequences of a single module failure along with the reliance on a single controller mean the network has no integral redundancy. High power systems based on this scheme would only be a logical choice if security of supply was of

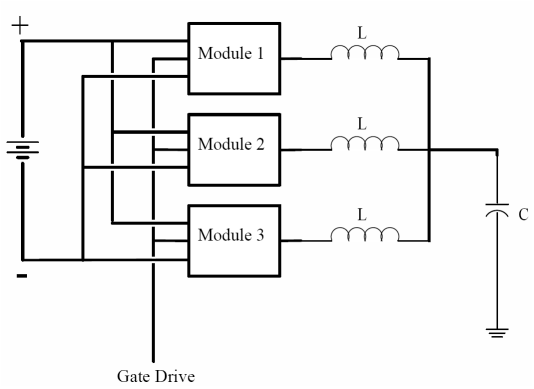


Figure 2.3 Soft Connection Topology Device Layout

low importance and the per unit cost of the controller was significantly higher than the cost of multiple modules. This is the opposite of the likely scenario.

There is nothing to prevent some segregation of modules in a directly connected system, such as the inclusion of module level fault protection and isolation, but this simply introduces many of the overheads of an actively paralleled system while failing to provide the benefits of full active paralleling.

2.3.2 Soft Connection

Soft connection is the term chosen to describe a network of modules in which an inductor is connected in series between the output of each module and the common output buss. Soft connection retains some of the advantages of direct connection (Single controller, simple control method) while mitigating some of the risks that make direct connection impractical. The series output inductor limits the slew rate of the differential current, greatly reducing the problems stemming from the minor differences in device characteristics described in the previous section. It also aids in balancing the AC component of the current through it's action as an impedance. Representative device layout in a soft connected topology is show in figure 2.3.

The simplicity of this method, combined with its potential high control bandwidth and the significantly reduced risks of problems due to minor parameter variations make it worthy of additional investigation. In the absence of supporting research from other sources, a theoretical case study was conducted as part of this thesis. The results, presented in chapter 3, indicate that soft paralleling is likely to be a reasonably effective method of coarse load sharing, but design tolerances in the construction of chokes and likely skew in switching impulses to the power devices combine to make it fairly unrealistic with regard to the level of system de-rating targeted by this research.

To improve current sharing, a common output choke can be used, the flux linkage between individual modules output currents acting to equalise those currents. This could dramatically improve the current sharing, but takes the complications of expanding a system or having a single product line to an extreme, not to mention the significant expense of the additional magnetics.

2.4 ACTIVELY PARALLELED SYSTEM TOPOLOGIES

Modules in an actively paralleled system modify the local output reference to maintain the module load at a level appropriate to its place in the network. To achieve this a variety of both module and system level feedback channels can be used, their exact number and nature dependent on the paralleling mechanism employed. While an actively paralleled system may also

benefit from the passive sharing mechanisms mentioned earlier, their action is secondary in level of influence and may be overridden if it doesn't comply with the actions of the active system. However, given the control resolution limitations imposed by the switching frequency, the passive sharing mechanisms are still vital for limitation of high frequency ($\frac{f_s}{2}$) circulating currents. The following topologies are presented in order of decreasing control structure distribution.

A control loop in which the output reference is based purely upon variables local to that inverter module cannot be employing an active paralleling algorithm as there is no data on which to act. The closest an active control scheme comes to this situation is in the case of simple output droop, in which only the voltage on the output bus is a global variable.

2.4.1 Output Drooping - Loosely Coupled Control

By far the most widely discussed in the literature on load sharing between paralleled inverters are those schemes in which only the output bus is required to be common. In this topology each module has its own controller and power flow is based on the variables measurable at the common bus. Load sharing is typically provided by a mimicry in the software control loop of the droop mechanism present in generator networks. The modified variable can be either the amplitude or frequency of the output voltage, specific control techniques common to this topology are discussed in the later section on control methods. The disadvantage of this method is that the output voltage changes with changing load, the magnitude of the change being proportional to the change in load and the accuracy of load sharing desired. Implementation of this algorithm essentially involves inserting a lossless impedance in the output of the system.

2.4.2 Networked Controllers - Closely Coupled Control

This topology involves several spatially isolated processors connected by a communications framework (analog, digital, or combinations of the two) and each driving a single associated power module. System load information is shared using this network, allowing each processor to regulate its local modules load in accordance with the system load conditions. Performance depends heavily on the communications network in place, and the control algorithm used. Each module needs independent sensing and control. There are a number of methods discussed later that seem to deliver performance sufficient to meet the demands of the development target. The high performance, combined with the modularity, maintainability, redundancy, and competitive production cost achievable, makes this a very promising topology. The majority of this thesis deals with development of a new algorithm intended for implementation on a platform of this type, however it is equally applicable to a single multichannel controller.

2.4.3 Single Multichannel Controller - Commonly Sourced Control

As for the networked topology, but instead of multiple processors sharing data via a network, a single processor monitors all sensing elements and generates all reference waveforms, implementing what could be a similar sharing algorithm to those suitable for networked control locally. This method does not include an external communication line in the control loop, which allows increased noise immunity and increased bandwidth. With many of the systems described later in this chapter and developed later in the thesis, the bandwidth of the sharing network is the limiting element in the bandwidth of the control response. However, if there were sufficient benefit in increasing this bandwidth, systems are already available that would allow the control loop bandwidth in a networked control system to exceed the switching frequency substantially. While it allows very high performance, this topology doesn't lend itself to modularity. The single processor core basically dictates a monolithic system, and spatial constraints on sensing and control lead run lengths will rapidly constrain system size. It could be a practical option

for a system requiring only a few paralleled elements to meet the required power rating, but all things considered a fully modular system is likely to be simpler and more cost effective in the long run; though modularity is likely to be at greater complexity and design cost in the short term.

2.5 CONTROL METHODS FOR ACTIVELY PARALLELED SYSTEMS

The active parallel control topologies mentioned above achieve a level of load sharing through passive characteristics, however their significant performance edge over the purely passive systems arises from the modification of the control algorithm to actively improve parallel load sharing. The algorithm must be compatible with the limitations of the system hardware topology, for instance a system topology in which the only common element between modules is the output buss cannot support a paralleling algorithm requiring the sharing of multiple variables, as the required communication framework does not exist. The algorithms presented in this section are drawn from previous research, as referenced. The conclusions drawn arise from juxtaposition of the experimental results presented, and consideration of the specific goals of this research.

The load sharing algorithms introduced operate in conjunction with the local voltage/current control loop. Those described below can be considered as operating with a generic voltage control loop, the internal specifics of which are significant to the final performance, but irrelevant to the particulars of the sharing algorithm. As mentioned earlier, the control algorithms for passively paralleled systems are by definition no different to those of stand alone systems. A review of appropriate local control algorithms was conducted in the process of the research, however it is somewhat tangential to the focus of this thesis. A brief summary of the voltage control loop used in the later design and test phase is presented in Appendix C.

2.5.1 Loosely Coupled Algorithms

The following algorithms are suitable for loosely coupled parallel systems in which only the output buss is shared. Each paralleled module has an independent controller which actively regulates its local power flow based on measurement of the output buss.

Linear droop

Conventional power sharing is based on drooping the related variable to indicate an increase in the quantity of that power type being transferred. The simplest of these involves a linear droop of both the frequency and amplitude, proportional to real and reactive power flow respectively.

$$\omega_i = \omega_{nominal} - m_p P \tag{2.4}$$

$$V_i = V_{nominal} - m_q Q \tag{2.5}$$

Implementation of these two equations would be all that is required to equalise load between multiple inverters, assuming the system output impedance satisfies $(X/R) >> 1$. Increasing P causes a reduction in power angle, reducing P. Likewise with V and Q. In either case the droop relationship leads towards equilibrium. The residual error is dependent on the error in voltage generation. There are several problems with the above system however, the first problem being the cause of the later problems. In the above equations, it is obvious that any load will result in a deviation of V and ω from their nominal values. A clever designer might pick the nominal values such that at typical load the outputs were at their ideal value, but this would still not prevent variations. Because the allowable deviation from nominal voltage and frequency in a power system is usually very small, the droop coefficients m_Q and m_P must also be very small. This

would not necessarily be a problem if a controller of extremely high speed and resolution were used and the system output bus was noise free, but obviously expecting such an environment is naive. In reality, the small coefficients lead to poor transient response, inaccurate power sharing, and compromised system stability, no different to the situation you would expect in any other area where a high gain proportional controller was attempting to regulate a non-linear or highly transient variable.

Given the huge benefits of the near total redundancy offered by droop based control, a solution to the above is extremely valuable. This solution would ideally avoid a trade off between voltage regulation and load sharing.

There has been a significant amount of research into micro-grid and distributed generation load sharing techniques using derivatives of these droop mechanisms, however the low bandwidth of the systems in comparison to those incorporating a dedicated communication network means they're uncompetitive in the context of this thesis, and as such are not discussed individually. They may however be of great value in highly distributed systems. A number of other loosely coupled systems in addition to those discussed below are presented in [1], [2], [3].

Transient droop

One of the problems with the purely linear frequency droop described above is that the transient response and steady state sharing are largely proportional to the steady state frequency and amplitude error. A droop algorithm designed to improve the transient response while reducing the steady state frequency error involves the following substitution

$$m \Rightarrow m_p + m_d \frac{s}{s + \tau^{-1}} \tag{2.6}$$

giving

$$\omega = \omega_{nominal} - m_p P - m_d \frac{s}{s + \tau^{-1}} P \tag{2.7}$$

This is a transient droop, where τ is the time constant of the transient droop action. Using a comparatively large transient droop coefficient allows the transient load sharing to be retained while reducing the proportional droop coefficient to reduce the steady state error. This ensures relatively accurate regulation under steady state conditions while offering improved active power sharing during load transients [4]. The stable frequency regulation is a significant improvement over the performance offered by the direct proportional relationship, but the transient response is still unsatisfactory.

In an effort to improve it, a more complex scheme founded on the same principles has been developed [5]. The feedback expressions used are

$$\phi_i = -m \int_{-\infty}^{t} P d\tau - m_p P - m_d \frac{dP}{dt} \tag{2.8}$$

$$V_i = V_{nominal} - nQ - n_d \frac{dQ}{dt} \tag{2.9}$$

Considering $\omega = d\phi/dt$ it is apparent that the steady state V and ω from these espressions coincide with those from the conventional method.

The experimental results and small signal analysis of the above presented in [5] illustrate significant performance improvements over conventional droop methods with regard to power sharing, however they do not address the level of variation in voltage or frequency. In any event, both of these systems still rely on an observable deviation from the nominal frequency, which violates the design criteria for the system this research aims to develop.

Frequency side band droop

In todays world of large rectifier loads, we really need to consider schemes that offer good sharing of not only the fundamental load component, but also the harmonics. One such scheme is suggested in [6]. Real power, reactive power, and distortion power are all used as control variables. The basis of this scheme is the superposition of a small amplitude synchronisation signal on the fundamental output bus waveform, the reference voltage changing from

$$v_{ref} = Vcos\omega t$$

to

$$v_{ref} = Vcos\omega t + V_{h1}cos\omega_q t + V_{h2}cos\omega_d t \tag{2.10}$$

ω_q and ω_d are derived from droop characteristics based on nominal frequencies of 90 & 130Hz and drooped according to the calculated direct and quadrature power components.

This leads to phase difference between modules at the indicated carrier frequencies which, according to the rules of power transfer, leads to a small active power flow between modules. This power is measured, and the fundamental voltage reference is adjusted to correct the indicated imbalance in power.

The experimental results given illustrate the system shares non-linear and transient loads adequately. The quality of sharing is dependent on the droop coefficients, once again accuracy must be traded off against stability and allowable distortion. The benefit compared to the previous methods is that the fundamental distortion is avoided. Issues of power quality may arise however, as the harmonic distortion on the output will increase through the use of this scheme. The transient performance is also still inadequate.

Synthetic output inductor and variable gain resonant controller

The most promising of the loosely coupled algorithms investigated uses a load sharing controller optimised to function with a resonant voltage control loop [7]. Low THD and good current sharing are simultaneously obtained by controlling the power angle through a LMS estimator, and by synthesizing a variable inductance in series with the output impedance of the inverter. The harmonic currents are shared by controlling the gain of the resonant controller at the selected frequency.

This system was developed in recognition of the fact that many high performance inverters employ resonant controllers to deliver a small voltage THD in the presence of non-linear loads.

A typical voltage controller based on a resonant controller can be written as

$$G_v(s) = K_p + \sum_k \frac{2sK_i}{s^2 + \omega_k^2} \tag{2.11}$$

where $\omega_k = k\omega$, $k = 1, 3, 2p + 1$, and K_p and K_i are the proportional and integral gains.

Such a controller has near infinite gain at the fundamental and selected harmonic frequencies, which leads to an output impedance approaching zero at these frequencies, assuming the cable impedance is near zero. As a result, conventional droop schemes such as those discussed previously will not function, as the resonant controller will act to zero their synthetic resistance, negating the droop action and allowing unconstrained circulating power flow. Essentially a resonant controller makes the system act like a voltage source at the CCP, clearly such a system would not be conducive to parallel load sharing.

The control technique proposed uses a a few techniques to solve the problem. The first involves the insertion of a real inductance between the point at which the voltage loop is closed and the CCP. This is kept to $X_L < 0.25\%$. This attenuates the noise due to the direct parallel connection

of the inverters, and also adds a very small inductance between the 'voltage sources'. This still represents a very small output impedance however, so to insert an impedance while retaining the low THD the output voltage is adjusted according to

$$\overline{V_i} = \overline{V_{oi}} - j\omega K_L \overline{I_i} \tag{2.12}$$

where

$$I_i = I_{Si} sin\omega t + I_{Ci} cos\omega t \tag{2.13}$$

The coefficient K_L is not fixed, but varies and acts as a virtual inductor in series with the output impedance of the inverter. We have therefore replaced the output impedance - previously ~ 0 due to the effect of the resonant controller - with $K_{total} = K_L + X_f$, where X_f is the impedance of the very small inductor between the closed loop voltage point and the CCP.

The load angle and amplitude are measured at the point of common connection, after the HF ripple filter (L_f), using an LMS based process. Once the load angle and amplitude are known, the reactive current is shared by varying the virtual inductance as a function of the reactive current while keeping the sinusoidal reference amplitude constant, while the phase is adjusted to achieve active current sharing.

The fundamental component of the voltage at the point of common connection is

$$v(t) = V sin(\omega t + \phi) = V_d sin(\omega t) + V_q cos(\omega t) \tag{2.14}$$

This can be expressed in matrix form as

$$v(t) = H(t) \cdot x$$

$$H = [sin(\omega t) \quad cos(\omega t)]$$

$$x = [V_d \quad V_q]^T$$

If G is the gain of the estimation process a clean signal can be extracted according to:

$$\hat{x}(n) = \hat{x}(n-1) + G[y(n) - H(n)\hat{x}(n-1)] \tag{2.15}$$

The amplitude of the fundamental voltage at the CCP is given by

$$V = \sqrt{V_d^2 + V_q^2} \tag{2.16}$$

The estimated signal is now a clean sine-wave that can be used to adjust the load angle and the output virtual inductance to achieve the desired load sharing while maintaining the low voltage THD offered by the resonant controller. For additional analysis and detail, refer [7].

The experimental results indicate very good current sharing in the presence of both linear and nonlinear loads, as well as total harmonic distortion in the region of $1 \rightarrow 2\%$, in keeping with the development projects goal of minimal output distortion.

2.5.2 Closely Coupled and Commonly Sourced Algorithms

The primary alternative to a loosely connected system employing one of the above algorithms is one in which the modules use a communications net entirely separate to the power buses to distribute information important to load sharing. This network could be implemented in software on a single centralised controller, or a variety of both analogue and digital data lines connecting multiple controllers can be employed. The similarity in possible dataflow means that the control algorithms for the two topologies are interchangeable.

In ideal circumstances, the results from a well designed networked system are far superior to those of a droop system, with near perfect load sharing whatever the load characteristics. The only real restriction is the bandwidth of the control loop

This system is not without weaknesses however. Firstly, the communication lines are potentially vulnerable to noise, restrict the spatial separation of the modules, and increase the required number of interconnections. For both the above reasons it is best to keep the modules close together, making this scheme more appropriate for single high power installations rather than large distributed generation schemes. The second major failing is that these systems are generally not truly redundant, if the comms net is compromised or the central controller fails then the entire array is lost. The risk of a catastrophic failure can be minimised by intelligent design. There is little additional risk in a network based scheme if a method of fault detection and isolation is included such that a failing module can be isolated from the rest of the system.

An important concept in closely coupled systems is the idea of a master and slave. A master controls itself, and can exercise a degree of global control. A slave controls itself to an extent, but also relies on an external master to provide global coordination. Closely coupled systems can fall into one of two categories.

- Master - Slave: In which a single master system coordinates the network of slaves and ensures they are operating so as to balance load between all modules in the network.
- Multiple Master: In which many master units cooperatively manage the network, each both listening and contributing to global load information and managing their local parameters so as to balance load.

Key points to consider in evaluating these topologies are:

1. Will the advantages of improved load sharing outweigh the costs in terms of lost reliability?
2. Can a suitable system be made that retains a high enough level of modularity to avoid an unnecessarily large product range?
3. Will the ability to share module attributes and array status with other modules allow an overall increase in reliability despite the possibility of lost redundancy?

To help in answering these questions it is necessary to examine common methods of communication based load sharing so the weaknesses and opportunities can be identified. These first three control structures are covered in more detail in [8]. In the figures associated with the following three control architectures V_{in} represents the supply voltage to the module, V_{out} is the output voltage from the system, and V_{ref} is the demand voltage set by whatever user interface/control reference generator is employed.

Inner loop regulation

The Inner Loop Regulation (ILR) structure has common output voltage feedback and compensator. The output of the compensator is a demand current to correct the error between the measured (V_{out}) and reference (V_{ref}) voltage. The ouput currents of each module are measured and error signals unique to each module are generated by a central current controller and used to adjust the reference current of each current controller. This scheme offers stable current regulation at the cost of reduced modularity and very low fault tolerance. A control line diagram is shown in fig 2.4.

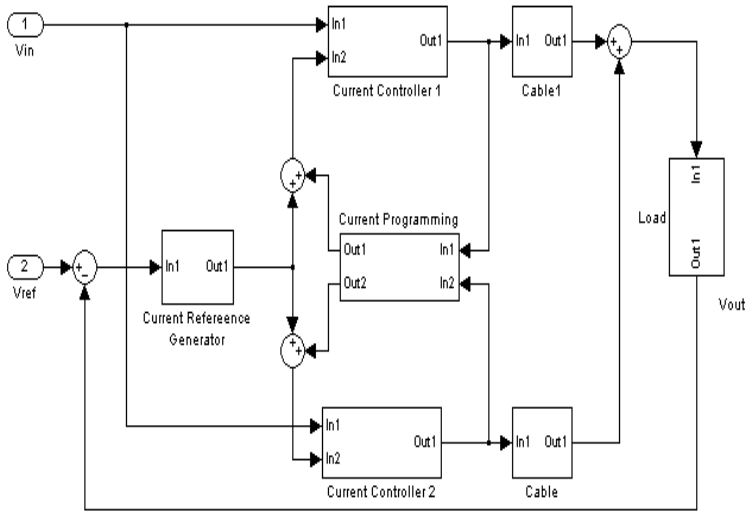


Figure 2.4 Load sharing using inner loop regulation

Outer loop regulation

The difference between Outer Loop Regulation (OLR) and ILR is that in OLR each module has an independent voltage feedback measurement and associated controller. Current references are still given by a central controller. A control line diagram is shown in fig 2.5.

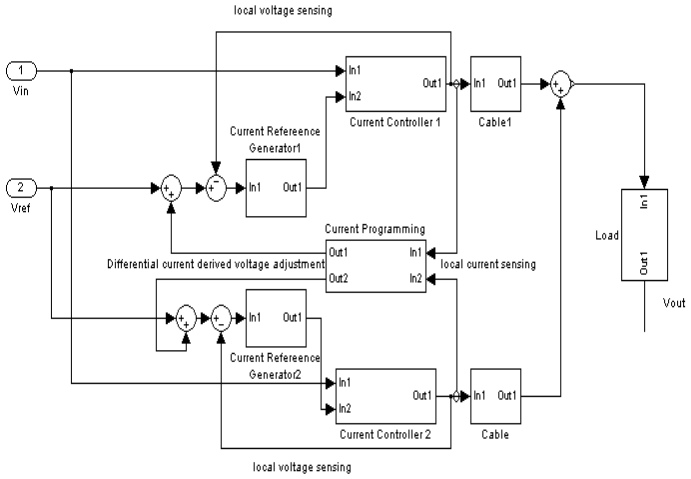


Figure 2.5 Load sharing using outer loop regulation

External controller

In this case a central controller collects all parameters and then sends voltage references to each module. Advantages are very good current sharing and output voltage regulation, as well as extremely high reliability unless the controller fails. Integration with a supervisory scheme is simple. Disadvantages are the large number of interconnections required, the reliance on a single controller, and the sharply defined maximum number of modules as limited by available processor I/O. Once the threshold is reached an entirely new processor is required to increase further. A control line diagram is shown in fig 2.6. Similar systems are discussed in [9].

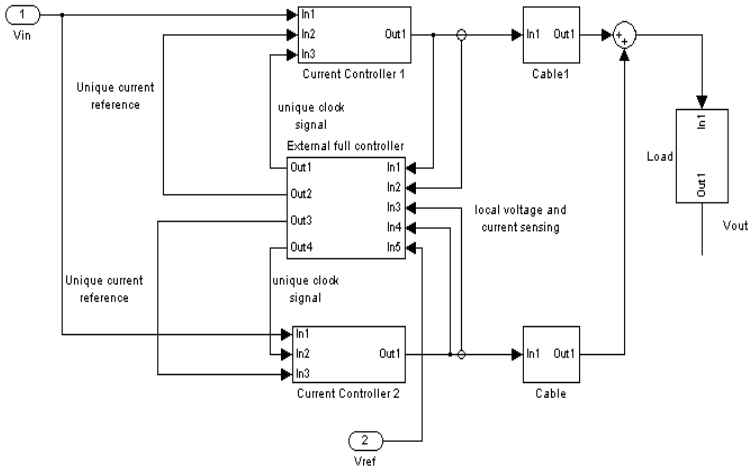


Figure 2.6 Load sharing using an External Controller

Active power and phase synchronism bus

This system, covered in [10], gives exceptional performance. The controllers are not common between modules either, so assuming a faulty unit does not corrupt the comms lines it is also a highly redundant system. The paper is extremely vague regarding the transfer functions used but most of the control blocks seem fairly generic.

Each module feeds its measured active power onto a common power signal bus via a resistance, and extracts the resistor summed average value from this bus for use as a power reference. The phase bus acts as a common reference, where each module synchronises itself with the bus using a phase locked loop.

An addition to the system is an adaptive controller to avoid errors due to hardware discrepancies (such as those discussed later in this research). This is worth noting, as it will probably be necessary in any multi element error integrating system to avoid saturation, and also has applications for the optimisation of any topology. Similar systems using current rather than voltage and phase are presented in [11], [12].

Multiple master with high speed sync line

Digital systems are capable of generating internal references with extremely high accuracy. Synchronising these references allows close synchronisation of the module outputs. A control scheme based on this theory is given in [13]. Clock drift between DSP's requires that the reference waveforms be re-synchronised roughly every period. More frequent synchronisation yields little advantage. Even with regular synchronisation there is a significant output voltage error. [13] claims that the error is due to differences in equivalent series resistance of the filter inductance. At this point in the paper the control system is single loop voltage feedback, so this could well be the case. Once a current feedback loop is included inside the voltage feedback loop, performance improves significantly. Hopefully the use of a high speed sync line will enable the modules to respond to any transient in a fairly similar manner (appropriate to their rating). Any long term trend towards an imbalance in load could be corrected using a comparatively low bandwidth load sharing line between controllers. No investigation is presented as to the bandwidth limitation. Similar systems are presented in [14], [15], [16], [17].

Digital multiple variable sharing network

No literature was found relating to active load sharing between parallel power modules using high speed data networks, so an attempt to outline the requirements and possible mode of operation of such a system is made by inference from existing systems. As mentioned earlier, the load sharing performance of a networked controller system will be primarily dependent on the data rate, and hence control loop sample rate, of the outer current control loop. Infinite sample rate would correspond to near perfect control, assuming a correspondingly large rate of response at the control loop output - physical system interface. The control methods discussed above use an analog communication bus. While this lacks the noise immunity and versatility of a digital bus, it does provide an extremely high bandwidth, leading to the very low sharing error shown. With a digital network, the effective sample rate of the control loop can be taken to be the rate with which the variable to be shared can be updated - the local control loop may run at a higher rate but the variables being used to control the load sharing will be undersampled. The rate at which the variables shared between modules are updated depends on three things.

1. The data rate of the network
2. The control method
3. The number of control modules

The reasons for the first limitation are obvious. The control method is significant because it influences how many variables must be shared over the network, for example in a master-slave configuration only the master will be publishing data onto the network, whereas in a multiple master system all controllers will be publishing. This leads to the third limiting factor, as if each controller must be allocated a fraction of the channel, then an increase in the number of controllers reduces the fraction of the channel available to a given controller.

Attempting to share all variables at high rate, such as in the analogue power/phase bus method, would require an extremely high data rate, and is essentially trying to emulate an analogue solution in a digital environment, a process to be wary of as in doing so advantages of the digital environment are often overlooked. Development effort should instead be focussed on development of lower rate data networks that build on the promising performance of schemes such as the waveform synchronisation method previously mentioned, and which make use of characteristics unique to digital systems such as very high accuracy of waveform generation and lossless information exchange.

2.6 SUMMARY

Technology that allows power semiconductor devices, and modules comprising systems of devices, to operate in parallel stably and with good load sharing without degradation of response is a key enabler for the penetration of power electronic systems into the high power, high bandwidth marketplace.

While a wide variety of potential control methods and topologies exist, the focus of this research will be on modular semi-independent networked controllers. Based on the literature review this is the topology most likely to deliver the goals of maintainability, performance, reliability, and modularity/scalability.

The specific control algorithm will be developed in the course of the research, and will be based on the following discussed control techniques:

- A multiple master control topology - This allows redundancy and hence high reliability, which was identified as a key requirement of the system.

- An improved variant of droop based load sharing drawing on the techniques introduced by the Active Power and Phase synchronism Bus method - This method delivered very positive results with regard to transient response, and unlike the loosely coupled algorithms did not result in a steady state deviation of the output from the nominal operating point.
- A high rate synchronisation line allowing high precision alignment of unmodified reference voltage waveforms - This minimises the voltage errors that lead to a load imbalance in the first place, and is also a key feature in a robust networked system, as it allows synchronous operation of other key functions such as starts, stops, ramp changes etc.
- A digital variable sharing network to optimise and tune module responses - Initial calibration to minimise load imbalance is important but very difficult to get exactly right and in any event is likely to drift over time. Online optimisation ensures the system remains able to operate at maximum utilisation, another key requirement of the development.

These methods in combination are expected to meet the performance criteria, and support the desired scalable system topology.

Chapter 3

PASSIVELY BALANCED PARALLEL SYSTEMS

3.1 INTRODUCTION

This chapter investigates the feasibility of connecting VSI modules in parallel with common gate drive control but separate output chokes with regard to the load sharing performance. The causes and effects of current sharing errors in passively balanced systems are identified, and based on the identified error sources both analytical and iterative error estimation methods are derived. This allows quick estimation of the level by which such a system would need to be derated to ensure reliable operation. The results also indicate the likely performance of the system with regard to the parallel module specification, and whether there is enough error present to justify development of active balancing technology.

3.2 SYSTEM TOPOLOGY

Passive paralleling is the term chosen to describe the process of paralleling when passive elements are responsible for the load balancing action. The passively paralleled system in this example is one in which a number of half bridge modules have their outputs connected by some inductance L to a common output bus, a topology termed 'soft paralleled' in this document. It is intended that this inductance will remove the system's susceptibility to small errors in device switching parameters and gate drive signal skew by suppressing large transient current flow between modules. A representative system is shown in fig 3.1.

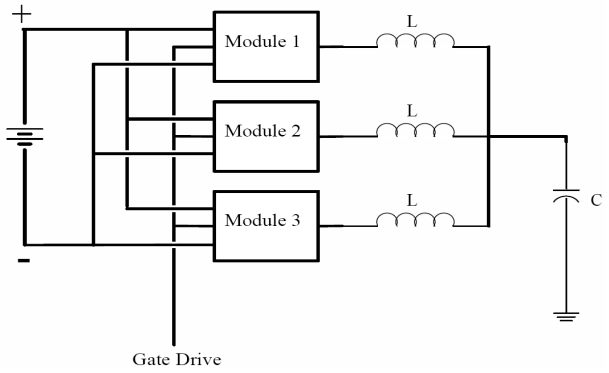


Figure 3.1 Soft parallel system topology

3.3 PASSIVE ELEMENTS CONTRIBUTING TO LOAD IMBALANCE

Most of the components used in a VSI have parameters specified as falling between some typical and maximum values. Parameters identified as significant are those likely to cause a differing on-state voltage drop/resistance, modulation index, and current slew rate. Parameters whose effect is rendered insignificant by the consideration of another component are ignored. The half bridge modules are assumed to be composed of IGBTs and power diodes.

3.3.1 Significant Parameters

The below parameters are those associated with the power stages of the paralleled modules that have been identified as likely to lead to differential intermodule voltages:

1. IGBT on-state voltage drop: This changes the effective bus voltage available, which changes the voltage at the output for a given modulation depth, giving the potential for a differential voltage. It has been modelled to include the devices on-state resistance as well as the fixed voltage drop across the semiconductor.

2. Diode on-state voltage drop: The mechanism and effects of variations in this parameter are identical to the above; the diode represents the current path when the device is turned off.

3. Gate drive pulse distortion: A distortion of the gate drive impulse changes the point at which the device switches and begins to conduct. This in turn changes the effective modulation index, which directly impacts the output voltage and gives potential for a differential voltage.

4. Output Inductor Reactance: This affects the output current slew rate, and so limits transient circulating currents caused by switching edge differences. It is also the primary AC impedance component which could result in a direct impact on power flow following common principles of voltage division across an impedance.

5. Inductor and conductor resistance: These change the output impedance of the modules on the network for both DC and AC voltage elements, leading to potentially differing current and hence power flows.

3.3.2 Assumptions

1. The DC Bus is either common, or regulated to a sufficiently high extent that variations between module DC Bus voltages are negligibly small.

2. Differences in trace inductance due to module buswork are insignificant in comparison to the deliberately inserted output inductance.

3. Differences in threshold voltages between IGBTs are no longer significant, as the tendency for a device with a lower $V_{Threshold}$ to carry a significant over-current during switch transitions is countered by the output inductors limiting of di/dt. The same is assumed to be true of switch transition differentials introduced by differences in lifetime.

4. All modules are at approximately the same temperature : this assumption is made to avoid the significant complications of thermal modelling of modules, and should be valid considering the common geometry and environment of modules. All devices used have a positive temperature coefficient, so any temperature variation as a result of device imbalances will aid in correct distribution of current. Thermal runaway is not a concern.

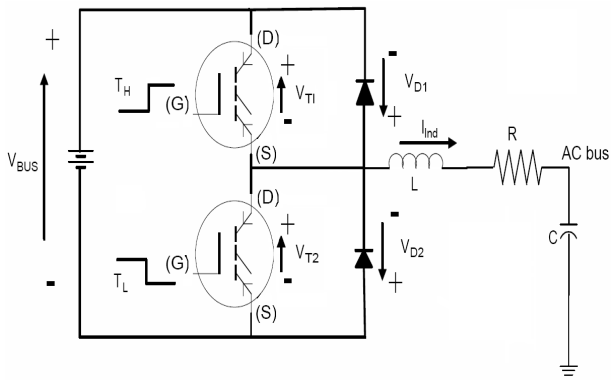


Figure 3.2 Inverter Module Voltage Differentials

Table 3.1 Instantaneous module output voltages

I_{ind}	T_{High}	T_{Low}	V_{Out}
0	0	0	$V^{+}_{Bus} + V_{D_1}$
1	0	0	$V^{-}_{Bus} - V_{D_2}$
0	1	0	$V^{+}_{Bus} + V_{D_1}$
1	1	0	$V^{+}_{Bus} - V_{T_1}$
0	0	1	$V^{-}_{Bus} + V_{T_2}$
1	0	1	$V^{-}_{Bus} - V_{D_2}$

3.4 ITERATIVE SOLUTION METHOD BY SIMULATION

For the purposes of testing the response under a variety of load and reference conditions an accurate Simulink model was developed. The development process was as follows

1. Identify the effective module output voltage for all switch and current direction conditions. I_{ind}, the inductor current direction, is defined as flowing into the common AC bus for $I_{Direction} = 1$, and out of the bus for $I_{Direction} = 0$. T_{high} and T_{low} are the the gate drive signals for the upper and lower half of the bridge respectively, a 1 indicating the IGBT is on.

2. Create a look-up table based on these values, using the inverter model shown in fig 3.2. This look-up table (Table 3.1) is implemented as a series of product blocks and logic gates. The constants and gains reflect the on-state drops and channel resistances of the diodes and IGBTs, combined with the nominal DC bus voltages relative to a virtual zero reference point halfway between the +ve and -ve rails.

3. Repeat the above process for as many modules as required, altering the look-up table parameters to reflect the desired device variation.

4. Apply the output of each module to a transfer function representation of output inductors, again with the transfer function reflecting the differences between modules in output impedance.

5. Sum the voltage derived current from the above process to give the net inductor current. Subtract from this the output current at the current capacitor voltage to give the capacitor current, and based on this capacitor current calculate the future capacitor voltage.

Table 3.2 Semiconductor Parameters - Eupec FF400R12KT3

Device	*Parameter*	*Typ*	*Max*
IGBT	V_{on}	$0.87V$	$1.35V$
IGBT	R_{DS}	$2.5m\Omega$	
Diode	V_{on}	$1.16V$	$1.66V$
Diode	R_{AK}	$1.23m\Omega$	

Table 3.3 Simulink AC test parameters

Module	*Device*	V_{on}	R_{on}
Low	T_1	$1.35V$	$2.5m\Omega$
Low	T_2	$1.35V$	$2.5m\Omega$
Low	D_1	$1.16V$	$1.23m\Omega$
Low	D_2	$1.16V$	$1.23m\Omega$
High	T_1	$0.87V$	$2.5m\Omega$
High	T_2	$0.87V$	$2.5m\Omega$
High	D_1	$1.66V$	$1.23m\Omega$
High	D_2	$1.66V$	$1.23m\Omega$

A MatLab model was developed based on the above theory and used to simulate the current waveforms that could be expected in a two module system in this configuration. Worst case parameter variations are used to gauge the possible extent of the problem.

3.4.1 Parameters

Having established the structure of the inverter model, parameters are added such that it represents the real inverter. Parameters were chosen so as to result in the maximum possible error in a two module system. Larger errors are theoretically possible in a system with more modules, but are unlikely. Another thing to note is that the the device variations that would combine to produce the maximum AC error are different to those that would combine to produce the maximum DC error. Peak AC error will occur with devices giving a greater effective V_{DCBus}. Peak DC error will occur with devices giving an offset V_{DCBus}. Pulse distortion by the gate drive modules will result in a DC current error, but will have no significant effect on the AC error. For clarity, it is ignored in this AC test.

The values in Table 3.2 are derived from the datasheet for the Eupec FF400R12KT3 IGBT module. Near peak current operation is assumed so the values corresponding to an operating temperature of 125^oC are used. The module values given in Table 3.3 are selected to give a maximum difference in effective V_{Bus}.

The output inductors are taken to be at the upper and lower limits of the envelope around the nominal value. The lower value is associated with the high current module. V_{Bus} is taken to be $566V$

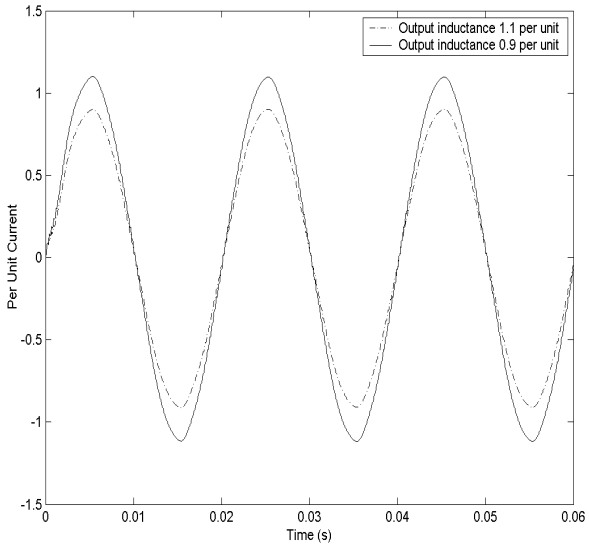


Figure 3.3 Current sharing - ±10% inductor error

3.4.2 Results

The module currents and associated inductor values are given in fig 3.3 and fig 3.4. In fig 3.3 the high inductance module is carrying $0.9p.u$ current, while the low inductance module is carrying $1.1p.u$. In fig 3.4 the high inductance module is carrying $0.95p.u$ with the low inductance module carrying $1.05p.u$. All waveforms have been lowpass filtered to remove switching ripple for clarity, this will have no effect on the apparent current distribution. These imbalances in current are directly proportional to the discrepancies in output inductance in both cases, with semiconductive device variations appearing to have no significant impact on AC current sharing.

3.5 ANALYTICAL SOLUTION METHOD

The previous results are strong evidence that the output inductor is the determining factor in AC current sharing. With DC current flow however, the impedance between modules is much lower and so even the small errors introduced by device dissimilarities could lead to significant current flow. The equations below are derived from the model in fig 3.2.

$$V_{out}(t) = \frac{mV_{Bus}}{2} + \Delta V^{+} + \Delta V^{-} \tag{3.1}$$

where m is the modulation index, V_{Bus} is the bus voltage, ΔV^{+} is the voltage error during positive current, and ΔV^{-} is the voltage error during negative current. If T_P is the period of the fundamental, then we can define the high and low switching periods (neglecting deadtime) as

$$T_H = (1+m)\frac{T_P}{2} \tag{3.2}$$

and

$$T_L = (1-m)\frac{T_P}{2} \tag{3.3}$$

which leads to the following expressions,

$$\Delta V^{+} = -V_{T_1}\frac{T_H}{T_P} - V_{D_2}\frac{T_L}{T_P} - (V_{Bus}+V_{D_2})\frac{T_{DT}}{T_P}$$

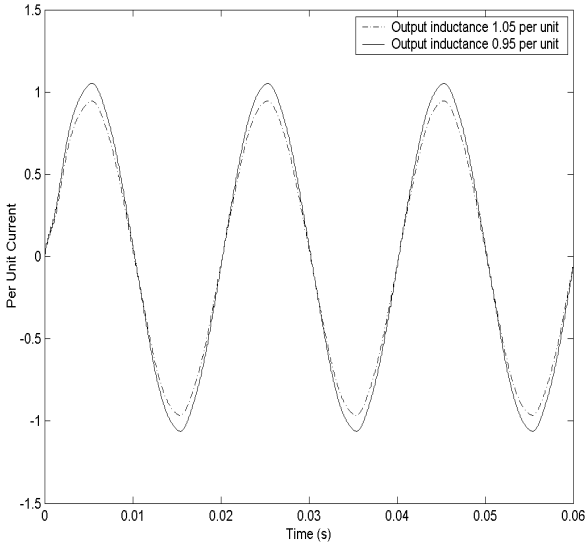


Figure 3.4 Current sharing - ±5% inductor error

$$+(V_{Bus} - V_{T_1} + V_{D_2})\frac{T_{H_{Warp}}}{T_P} \tag{3.4}$$

$$\Delta V^- = +V_{T_2}\frac{T_L}{T_P} + V_{D_1}\frac{T_H}{T_P} + (V_{Bus} + V_{D_1})\frac{T_{DT}}{T_P}$$

$$-(V_{Bus} - V_{T_2} + V_{D_1})\frac{T_{L_{Warp}}}{T_P} \tag{3.5}$$

where T_{DT} is the deadtime between high and low switching pulses, $T_{H_{warp}}$ is the skew between modules for the high switching pulse, and $T_{L_{warp}}$ is the skew between modules for the low switching pulse.

Rewriting in terms of the modulation index m gives the following

$$\Delta V^+ = -\left[\frac{V_{T_1} + V_{D_2}}{2} + \frac{V_{T_1} - V_{D_2}}{2}m + \frac{V_{Bus}(T_{DT} - T_{H_{Warp}})}{T_P}\right] \tag{3.6}$$

$$\Delta V^- = \left[\frac{V_{T_2} + V_{D_1}}{2} + \frac{V_{D_1} - V_{T_2}}{2}m + \frac{V_{Bus}(T_{DT} - T_{L_{Warp}})}{T_P}\right] \tag{3.7}$$

Close observation will reveal that the diode voltage has been neglected in the final terms of the above two expressions. Given the likely magnitude of V_{Bus} its effect will be negligible.

The DC current is found from the average voltage across the output inductor. The common AC output bus is modelled as an ideal AC source, which by definition has an average voltage of zero. Therefore the average voltage across the inductor is the average voltage at the VSI output terminal. This can be found by integrating the error voltage over one period. To aid in the calculation of this error two new terms, $S_1(\theta)$ and $S_2(\theta)$. $S_1(\theta)$ plus $S_2(\theta)$ equals 1, the weighting varied to replicate the effect of a DC current on the ratio of positive current to negative current at the output.

$$\Delta V = S_1(\theta)\,\Delta V^+ + S_2(\theta)\,\Delta V^- \tag{3.8}$$

$$V_{DC} = \frac{1}{2\pi}\int_0^{2\pi} \Delta V d\theta, m = m_A sin\theta \tag{3.9}$$

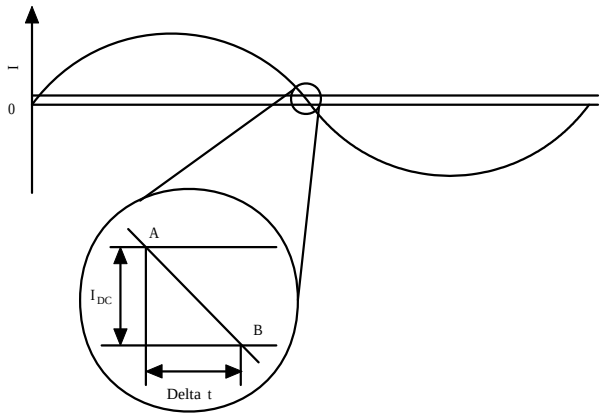


Figure 3.5 I_{DC} effect around zero crossing

Treating $S_1(\theta)$ and $S_2(\theta)$ as variables, evaluation of the integral gives the following result

$$V_{DC} = S_1(\theta)\left[-\frac{V_{T_1}+V_{D_2}}{2} - \frac{2}{\pi}m_A\frac{V_{T_1}-V_{D_2}}{2}\right.$$
$$\left.-\frac{V_{Bus}(T_{DT}-T_{H_{Warp}})}{T_P}\right] + S_2(\theta)\left[\frac{V_{T_2}+V_{D_1}}{2}\right.$$
$$\left.+\frac{2}{\pi}m_A\frac{V_{D_1}-V_{T_2}}{2} + \frac{V_{Bus}(T_{DT}-T_{L_{Warp}})}{T_P}\right] \tag{3.10}$$

We now need to define $S_1(\theta)$ and $S_2(\theta)$ such that the DC current offset has the correct effect mathematically on the current direction. From fig 3.5 we can see that a DC current equal to +5% of the peak AC current prolongs the +ve period by $0.05\pi\frac{1}{f}$ and truncates the -ve period by the same amount. Based on this, the following definitions hold for small DC current flow

$$S_1(\theta) = 0.5 + \frac{I_{DC}}{\pi I_{Peak}} \tag{3.11}$$

$$S_2(\theta) = 0.5 - \frac{I_{DC}}{\pi I_{Peak}} \tag{3.12}$$

Substituting these terms into equation 10 and rearranging the result gives

$$V_{DC} = \frac{V_{T_2-T_1}+V_{D_1-D_2}}{4} + \frac{V_{D_1+D_2}-V_{T_1+T_2}}{2\pi}m_A$$
$$+\frac{V_{Bus}[T_{H_{Warp}}-T_{L_{Warp}}]}{2T_P} + \frac{I_{DC}}{\pi I_{Peak}}\left[\frac{-V_{T_1+T_2}-V_{D_1+D_2}}{2}\right.$$
$$\left.+\frac{V_{D_2-D_1}+V_{T_2-T_1}}{\pi}m_A - \frac{V_{Bus}[2T_{DT}-T_{H_{Warp+L_{Warp}}}]}{T_P}\right] \tag{3.13}$$

Entering the parameters of the components used into the above equation will give the DC current. In the following example, values have been selected from the extremes of the range and combined in such a way as to give the maximum error voltage.

Example: Worst case DC current flow

Parameters from Eupec FF300R12KT3 IGBTs, through 5mΩ output impedance.
$V_{Bus} = 566V$
$V_{T_1} = 1.7V$
$V_{T_2} = 2.15V$
$V_{D_1} = 2.15V$
$V_{D_2} = 1.65V$
$T_{DT} = 2\mu s$
$T_P = 250\mu s$
$R_L = 5m\Omega$
$T_{H_{Warp}} = +100ns$
$T_{L_{Warp}} = -100ns$

$$V_{DC} = \frac{0.45 + 0.5}{4} + \frac{-0.05}{2\pi} + \frac{V_{Bus}[(100ns) - (-100ns)]}{500\mu s}$$

$$+\frac{I_{DC}}{\pi I_{Peak}}\left[\frac{-3.85 - 3.8}{2} + \frac{-0.5 + 0.45}{\pi} - 9\right]$$

$= 0.4559 - 0.014I_{DC}$
$\Rightarrow I_{DC} = 200(0.4459 - 0.014I_{DC})$
$\Rightarrow I_{DC} = 24.0A = 8.3\%$

In order to check the above equation, a module with the same parameters was modelled in Simulink. Two different methods were used. The first, a version of the Simulink model used for AC sharing estimation with the device values modified to give a DC offset, gave a DC current error of $23.1A$. The second, a simplified Simulink model in which the device errors are represented by a constant voltage error with a feedback term to simulate the correcting effect of current direction differences, gave a DC error of $20.5A$. Of the three methods, the full inverter model based system is probably the most accurate as it takes current magnitude into account when calculating voltage drops across the semiconductors, but the three agree to within a small enough margin that using any of them will give a useful result. The analytical method is certainly the fastest and simplest.

3.6 PRACTICAL IMPLICATIONS OF RESULTS

The required derating of the soft paralleled system is determined by finding the extent by which the current could exceed its intended peak value as a result of imbalance. The ratable power of the module is the actual capacity of the module minus this possible excess current. This ensures that any module carrying both its full rated load and the maximum error current will still be operating within its performance envelope. From the calculation in the previous sections example, worst case device errors using the Eupec FF300R12KT3 IGBT will result in 4.5% current imbalance. The worst case error due to pulse warping results in an additional 4% current imbalance. Any variation between inductors in the output filters will result in an additional circulating current proportional to the difference between inductances. This gives a total error of 8.5% + inductor error (p.u). The probability of encountering such an extreme set of device parameters **and** having them distributed in such a way as to produce maximum offset within one module is probably very low, but the statistical likelihood is not considered in this paper. The prediction is that with a ±5% inductor variation the total circulating current will be under 10% in the configuration discussed in this paper.

3.7 ADDITIONAL PROBLEMS WITH PASSIVE PARALLELING ARCHITECTURE

This study has assessed the potential worst case circulating current flows resulting from readily estimated variations, however it still assumes largely ideal system distribution and does not consider fault conditions and component degradation with time. These associated issues are discussed briefly in the interests of completeness.

3.7.1 Intermodule Resistance

The DC current flow is largely defined by the resistance of the conductive path between modules. This is assumed to be fixed in the analysis to allow a consistently calculable result. The resistance in an actual system is extremely difficult to determine in advance by design, as a result is very difficult to control. The symmetry of resistance in a final product could be significantly different to what was intended; the effect on current flow as a result is obvious from inspection of the derived equations in the previous sections.

3.7.2 Gate Drive Pulse Fidelity

The analysis makes allowance for variations in the rate of switching device response to gate drive pulses, but does not consider other elements in the gate drive path likely to contribute further distortion. Isolation, level shifters, gate drivers, and even stray line capacitance most likely all add additional variation between modules. The level of variation is likely to increase with device ageing, and even if the change with age is symmetrical it will lead to major complications when a new modules is substituted for a faulty one.

3.7.3 Transient and Fault Current Management

Currents in physically large structures are very hard to manage during transients and faults. Multiple low impedance paths exist, and are unlikely to be independently monitored by any means other than last ditch protection mechanisms such as desat. Potential undetected fault currents are very large, and difficult to fuse against.

3.7.4 Failure Response

Failure mechanisms of large tightly coupled structures are often catastrophic. The ability of a failed module to corrupt the control of other modules coupled with the absence of a mechanism for isolation of a faulty module means that any failure is likely to be severe. Redundancy is zero.

3.8 SUMMARY

Paralleled VSI modules with common control signals, individual output chokes, and a common AC output bus should have a maximum circulating current in the region of 10% for inductor variations of $\pm$ 5%. This makes soft paralleling a viable method of providing high power VSI systems if the system can justify the cost of a 10% margin in installed power capacity to allow for circulating current. However, it suggests there is the potential for a significant gain in $\frac{kW}{\$}$ if an active system capable of eliminating the error is developed. Also, a system with common gate drive signalling and a requirement for small errors between inductors will not be suited to operation within a redundant system, will not be easily repairable, and will not allow the same opportunities for rationalisation of product range.

Chapter 4

DIFFERENTIAL DROOP ACTIVE CONTROL ALGORITHM DEVELOPMENT AND PROOF OF CONCEPT

4.1 INTRODUCTION

The review and investigation of the previous two chapters illustrated the serious limitations of passive methods of paralleling and also identified flaws in the existing methods of active paralleling. A new (or at least modified) active paralleling method is necessary to meet the requirements of the design brief. This chapter details the development of the active paralleling control algorithm, which is a derivative of the techniques identified in the literature review. An innovative droop variant, termed 'Differential Droop' is introduced and the benefits explained. The communication requirements of a differential droop based system are investigated, with an emphasis on methods of reducing the required bandwidth without compromising the end result.Simulink models are used to test the effectiveness of the developed methods. The basic algorithm is then proven in a physical system consisting of a single module operating in parallel with a low impedance voltage source.

4.2 THE DIFFERENTIAL DROOP ALGORITHM

As mentioned in chapter two's review and detailed in Appendix A, conventional droop based load sharing mechanisms operate by reducing the amplitude of the voltage reference waveform in response to a measured increase in module load. The disadvantage of this method is that the output voltage changes with changing load, and furthermore the more accurate the desired load sharing, the bigger the required change. Essentially by implementing this algorithm you are inserting a lossless impedance in the output of the system. No power is dissipated but a voltage drop relative to the nominal voltage occurs proportional to the output current.

Differential droop operates in a similar manner to conventional droop, however the output varies only in response to the differential load term, the common load term does not result in a change in voltage. The advantage of this is obvious; so long as the load is balanced there will be no change in output voltage control term with a load increase.

4.2.1 Algorithm function

The differential load term is the difference between the nominal local load and the actual local load. The nominal local load is the load that would result in all modules carrying the same load with respect to their power handling capacity. The instantaneous reference voltage term for a given module resulting from application of the differential droop algorithm is

$$v_{ref} = v_{nominal} - G_{Droop}.(i_{local} - i_{nominal}) \tag{4.1}$$

where G_{Droop} is the gain of the differential droop response loop, $v_{nominal}$ is the target output voltage, i_{local} is the local output current, and $i_{nominal}$ is given by

$$i_{nominal} = \frac{v_{nominal}}{X_{Out}} . \frac{P_{module}}{P_{system}} \tag{4.2}$$

where P_{module} and P_{system} are the rated power handling capacities of the module and the entire system respectively, and X_{Out} is the output impedance seen by the entire system. The total output current $\frac{V_{nominal}}{X_{out}}$ is comprised of all the local currents,

$$i_{out} = \sum_{1}^{n} i_k$$

where n is the number of modules in the system and i_k is the module current given by

$$i_k = i_{k.nominal} + \Delta i_k$$

Assuming identical power ratings for each module, $\frac{P_{module}}{P_{system}}$ becomes $\frac{1}{n}$, which gives

$$i_{k.nom} = \frac{v_{nom}}{X_{out}} \frac{1}{n}, k = 1, 2, ..., n \tag{4.3}$$

The following is therefore true.

$$i_{out} = \sum_{1}^{n} i_k = \sum_{1}^{n} i_{k.nom}$$

$$\Rightarrow \sum_{1}^{n} \Delta i_k = 0$$

The resultant output voltage is given by the average voltage of all modules,

$$v_{output} = \frac{n.v_{nom}}{n} - \frac{G_{Droop}}{n} \sum_{1}^{n} \Delta i_k = v_{nom} \tag{4.4}$$

proof that independent modules can theoretically share load using a differential droop based method without affecting the output voltage waveform.

4.2.2 The Significance of Communications Delay

The complication introduced by differential droop is that the nominal current must be known by each module. In the system envisaged, comprising multiple equally rated modules, the nominal current is the same as the average current. The average current is not a readily available variable, and must be derived by one of the two following methods.

1. Measurement of the total output current and division of the resulting measurement by the number of modules in the system.

2. Measurement of each individual module current, and calculation of the average.

Measurement of the output current directly is non-ideal as it requires an additional (and potentially colossal) current sensor, as well as introducing a potential single point of failure. Measurement of each individual modules current avoids both the pitfalls of the previous method, but requires that the module currents be published onto some form of system communication

network. As a result, a delay will be introduced into the control feedback loop to allow time for the information to be distributed and collated. Before continuing with a communication network based differential droop system, the significance of this delay must be determined to be sure such a system is feasible at the delays likely to be encountered.

The differential current term with consideration of communication delay becomes

$$\Delta i = i_{out}t - i_{avg}(t - dly)$$

For a linear load drawing only 1st harmonic the error will therefore be

$$\Delta i = I_{pk} \sin \omega t - I_{pk} \sin(\omega(t - dly))$$

which for low values of delay is approximated by

$$\Delta i = I_{pk}.dly.\omega \cos(\omega(t - dly))$$

For a $50hz$ system operating with an uncorrected communications delay of $500\mu s$ the error term due to communications delay will therefore be

$$\Delta i_{dly} = I_{pk}.500\mu.100\pi.cos(\omega(t - 500\mu s)) = 0.157 I_{pk} cos(\omega(t - 500\mu s))$$

This is a 16% current error at the fundamental frequency but with 85.5^o leading phase error. It is important to realise two key differences in the effect of this error term compared to the error term resulting from a module load imbalance, namely

1. This error term does not result from a load imbalance between modules and a droop action in response to the error will not result in a load imbalance between modules as all modules are seeing the same error and drooping in the same way.

2. This error term does **not** sum to zero over all modules, and so the output voltage **will** change as a result of it. The magnitude of this effect is shown below.

$$v_{output} = \frac{n.v_{nom}}{n} - \frac{G_{Droop}}{n} \sum_{1}^{n} \Delta i_k = v_{nom} - G_{Droop} I_{pk}.dly.\omega \cos(\omega(t - dly)) \qquad (4.5)$$

This gives a rough approximation of the final output, but the error is a result of the feedback loop, so an iterative solution is required for good accuracy. A MATLAB m-file was written to provide the iterative solution, this is used to generate the results below.

For a $50hz$ system running at $1pu$ load into a purely real impedance with a $500\mu s$ communication delay and a $0.2pu$ differential droop term, the output voltage would be

$$V_{out} = V_{pk} \sin \omega t - V_{pk}.(0.2 \times 0.157). \cos(\omega(t - dly)) = V_{pk} \sin \omega t - V_{pk} 0.031 \cos(\omega(t - dly))$$

by the once off calculation method, which by vector addition gives a resultant output voltage of

$$V_{out} = V_{mag} \sin(\omega t - \theta_{dly})$$

where V_{mag} is given by

$$V_{mag} = \sqrt{[V_{pk} - V_{pk} \times 0.031 \times \sin(\omega.dly)]^2 + [V_{pk} \times 0.031 \times \cos(\omega.dly)]^2}$$

and θ_{dly} by

$$\theta_{dly} = \tan^{-1} \frac{V_{pk} \times 0.031 \times \cos(\omega.dly)}{V_{pk} - V_{pk} \times 0.031 \times \sin(\omega.dly)}$$

resulting in

$$V_{out} = 0.9956 V_{pk} \sin(\omega t - 0.0312)$$

Using matlab to compute an iterative solution the result is

$$V_{out} = 0.9946 V_{pk} \sin(\omega t - 0.0309)$$

This result is within the tolerance set out for maximum output voltage distortion, so the design is suitable with regard to communications delay.

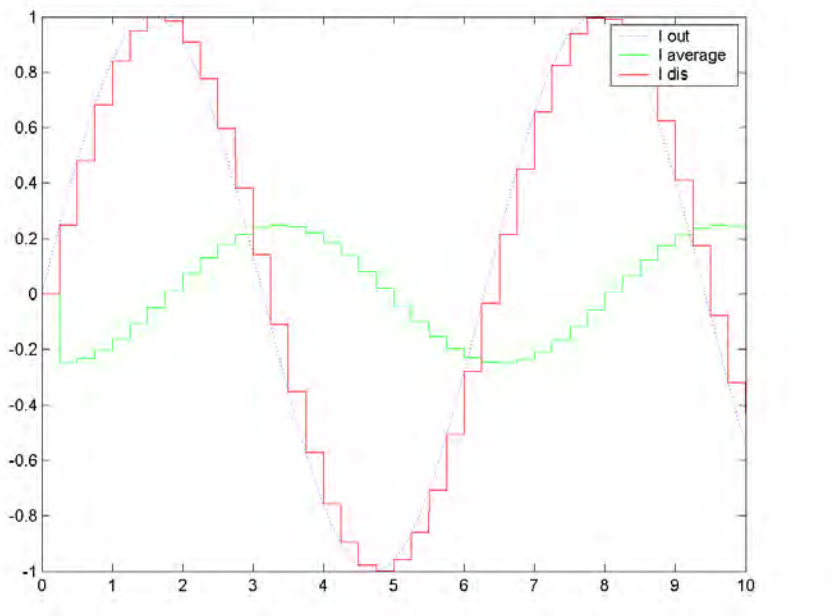


Figure 4.1 Actual vs Quantised waveform

4.2.3 Discretisation error

Discretization is a fundamental characteristic of digital systems. The communications delay is caused not by a propagation delay within the communications line, but by the fact that a given data packet, comprising one variable, takes some significant time to be transmitted, and there may be several such packets to be sent. Sending all the packets takes the delay time. Furthermore, the line does not become available for transmission of additional data until the end of that delay period, and it will take another delay period before the new sample is available. The point being that the averaged current will not be a continuously varying value, or even discretized to the system sample rate, but will be discretized to the delay rate. The effect of this can be calculated as follows.

$$\Delta i_{dis}[k] = i_{out}[k] - i_{avg}[k]$$

Fig 4.1 shows the two waveforms, $I_{average}$ and I_{out}. The average difference between these two waveforms over one delay period can be calculated as follows

$$\Delta i_{dis_{k1\rightarrow k2}} = \frac{(i_{out}[k2] - i_{out}[k1])}{2}$$

$$i_{out}[k2] - i_{out}[k1] = \frac{d}{dt} i_{out}[k + \frac{dly}{2}] \times dly$$

so

$$\Delta i_{dis_{k1\rightarrow k2}} = \frac{\frac{d}{dt} i_{out}[\frac{k1+k2}{2}] \times dly}{2}$$

Therefore under the same system conditions described in the previous section, the resulting error due to discretization will be

$$\Delta i_{dis} = \frac{I_{pk}.500\mu.100\pi.cos(\omega t - \frac{500\mu s}{2})}{2} = 0.079 I_{pk} cos(\omega t - 250\mu s)$$

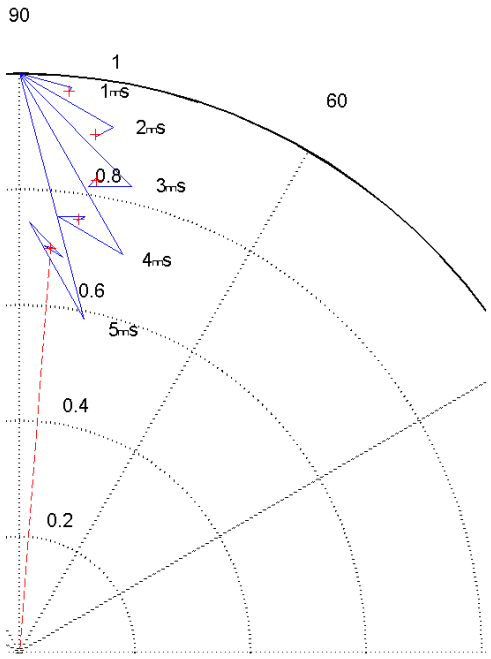


Figure 4.2 Iterative solution for delay effect

This produces a voltage error in the same way as the communications error did, the more accurate MATLAB iterative result being

$$V_{out} = 0.9986 V_{pk} \sin(\omega t - 0.0156)$$

As the two errors arise from the same source, the communications bandwidth limitation, it's sensible to combine their effects into a single expression.
For a delay of $500\mu s$ and droop gain of $0.2p.u$ the resulting output voltage is

$$V_{out} = 0.9928 V_{pk} \sin(\omega t - 0.0464)$$

The error increases rapidly with increasing delays. Figure 4.2 shows the results of MATLABs iterative solution method for delays of $1ms \rightarrow 5ms$. The red dotted line is the output voltage phasor for the $5ms$ case, being a voltage of

$$V_{out} = 0.6997 V_{pk} \sin(\omega t - 0.0779)$$

This is obviously an unacceptable result. At delays that large, the linearisation of the model is no longer accurate however, it is used as an example simply to illustrate the possible severity of the problem. At a smaller delay, say $1ms$, the result is

$$V_{out} = 0.9724 V_{pk} \sin(\omega t - 0.0884)$$

which is still a significant error, and this at a communications rate which will later be revealed as close to the maximum we can expect to achieve using a simple sharing method over the eCAN with 10 modules on the network. We could halve the droop coefficient to $G_{Droop} = 0.1$ which would result in an output of

$$V_{out} = 0.9870 V_{pk} \sin(\omega t - 0.0448)$$

but doing so would reduce the intermodule impedance and worsen sharing. Error compensation is a potentially attractive option.

4.2.4 Error Compensation

The errors introduced by the communications delay and quantisation of sensed current can be dealt with by adding additional feedforward components to the control loop. Instead of implementing this from the outset however it makes sense to assess the severity of the problem first. If sharing is sufficiently good that a low droop coefficient is reasonable then the error is negligible and compensation is unnecessary. Small steady state errors will be removed by the integral component in the voltage control loop.

4.3 PERFORMANCE UNDER SIMULATION OF DEVELOPED LOAD SHARING MECHANISM

The focus of this section is first to prove by simulation that differential droop causes modules to stably and effectively share current in the presence of factors contributing to module load imbalance. Proof of concept simulation will be done assuming unlimited available sharing bandwidth and consequently an ideal sharing rate. The available bandwidth will then be restricted to that available using the CAN ($1MBit/s$) and the performance reevaluated at this lower rate.

In recognition of the tight bandwidth constraint, some alternative methods of determining the key variable for controller load distribution, the total system load, were developed. These involve the sharing of only key elements of each modules local load conditions, these key elements being reconstructed by each module after collation to give the global load. Brief details of these alternatives are presented in Appendix B.

All simulations are based on a symmetric 3 module system with errors in real output impedance and reference voltage applied to provoke an imbalance so the correction mechanism can be evaluated. It must be emphasized that this is merely a convenient method of introducing an error term and unlikely to be a source of error in reality considering the accuracy with which digital references can be generated. In reality the primary source of error is likely to be error in external measurement of variables such as the output voltage, bearing in mind that this system uses closed loop control. A block diagram level schematic of the system is shown in fig 4.3 including the scaling errors used.

All results given exhibit a startup disturbance. This is caused by initial conditions in the model and is essentially irrelevant other than to indicate the rate of divergence in unstable systems, which is of minimal interest at any rate as our acceptance criteria for stability is simple pass/fail.

4.3.1 Ideal Intermodule Communication Bandwidth

The effect of the differential sharing system will be proven by modelling the above system first with no droop, then with droop, then with differential droop with the sharing based on ideal rate communications. The PWM based output stage has been removed from the simulation at this point to make the results clearer.

The results in fig 4.4 are for the uncompensated system. Sharing is obviously hopeless, the only reason there is any balancing action at all is that the current slew rate is limited by the output inductor, and peak current limited by a saturation process in the control loop. This system is equivalent to connecting three different voltage sources together through a near zero impedance. There is no way it would ever work. It is included here only to facilitate a demonstration of the effectiveness of droop based sharing in an otherwise identical system.

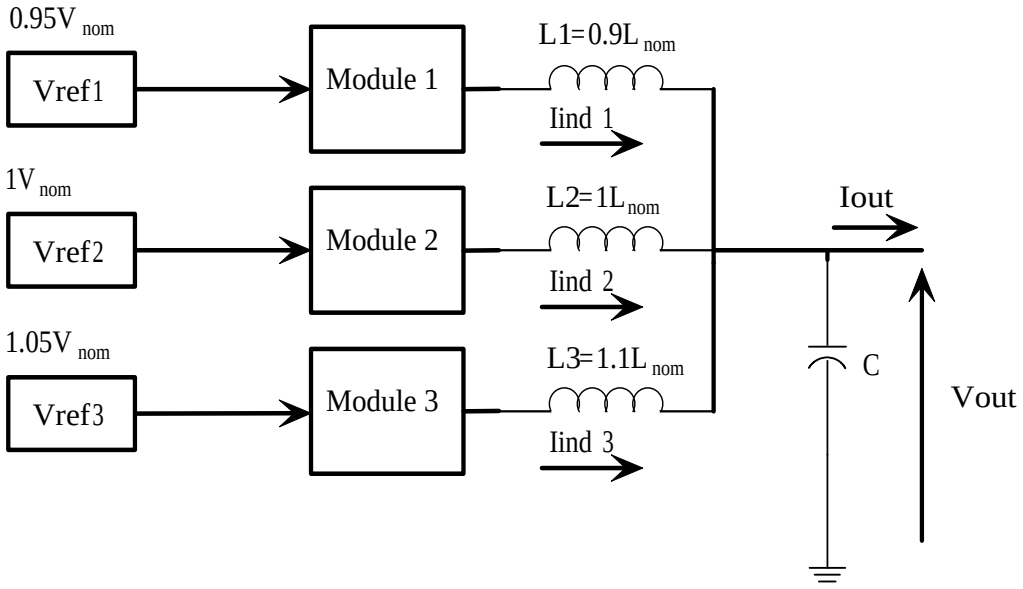


Figure 4.3 System topology for simulated system

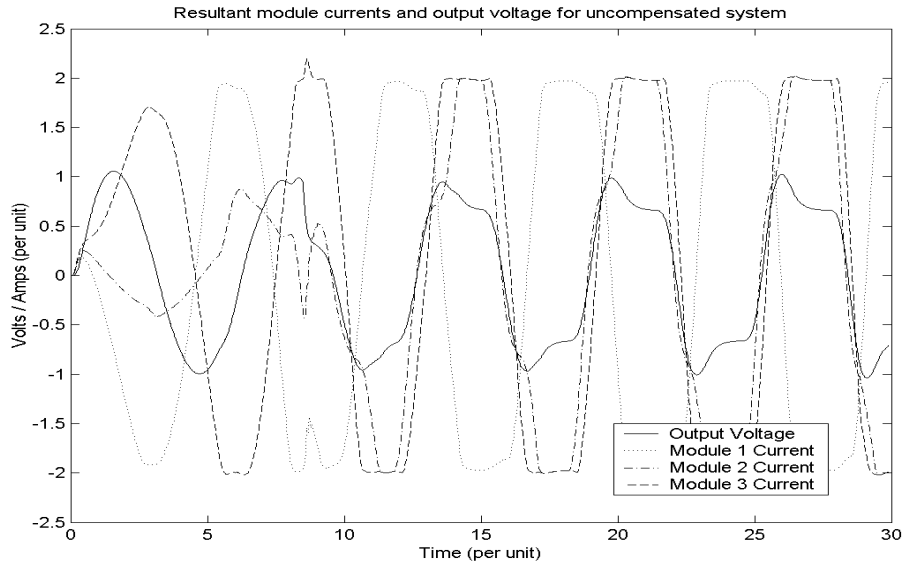


Figure 4.4 Results for uncompensated system

The simulation results shown in fig 4.5 are for a droop based system with a droop coefficient $G_{droop} = 0.2$. The non-differential droop mechanism is equivalent to inserting a lossless resistor of (in this case) $0.2.pu$ resistance in the output of each module. Theory indicates that this method applied to equalise a system with total voltage reference terms of $0.95V$, $1V$, and $1.05V$ respectively will result in a current imbalance as follows;

- The nominal module current is $1.pu$ by definition, but because the output voltage droops with increasing load, for a $1.pu$ load the output current will be

$$I_{out} = V_{avg} - 0.2I_{out} \Rightarrow I_{out} = \frac{1}{1.2} I_{nom} = 0.833 I_{nom} = 0.833.pu$$

- The $0.95V$ module will run at

$$(1 - 0.95) * 0.2 = 0.25 \Rightarrow 25\%$$

  below average module current

$$\Rightarrow I_{out:0.95Vnom} = 0.6247.pu$$

- The $1V$ module will run at

$$(1 - 1) * 0.2 = 0 \Rightarrow 0\%$$

  below average module current

$$\Rightarrow I_{out:Vnom} = 0.833.pu$$

- The $1.05V$ module will run at

$$(1 - 1.05) * 0.2 = -0.25 = -25\%$$

  below average module current

$$\Rightarrow I_{out:1.05Vnom} = 1.041.pu$$

Fig 4.5 clearly shows the agreement of the theory with the simulation. Note the significant deviation of the voltage from nominal levels characteristic of non-differential droop mechanisms.

Introducing the global current term for comparison transforms the droop system into a differential droop system. The theory for a system operating without a sharing delay, using $G_{droop} = 0.2$ as the differential droop coefficient, and running with introduced voltage reference errors of $\pm 5\%$ on two of the three modules respectively is given below.

The output should now be drooping based only on the average differential term (theoretically zero), so the output voltage under full load should remain at the nominal output voltage. This can be proven by a nodal analysis of the system.

$$V_{out} = \begin{vmatrix} -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{vmatrix} . \begin{vmatrix} i_1 \\ i_2 \\ i_3 \end{vmatrix} \times 0.2 + \begin{vmatrix} 0.95 \\ 1 \\ 1.05 \end{vmatrix}$$

Row addition of the above gives

$$3.V_{out} = \begin{vmatrix} 0 & 0 & 0 \end{vmatrix} . \begin{vmatrix} i_1 \\ i_2 \\ i_3 \end{vmatrix} \times 0.2 + 3$$

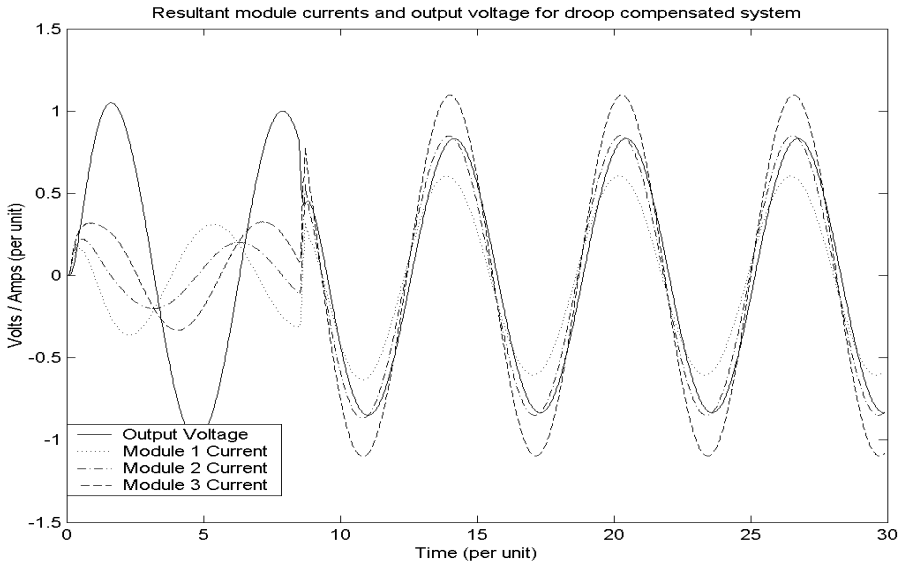


Figure 4.5 Results for droop compensated system : $G_{Droop} = 0.2$

$$\Rightarrow V_{out} = 1$$

Applying Kirchoffs voltage law at the output gives

$$V_{out} = I_{out}.X_{out} = (i_1 + i_2 + i_3).\frac{1}{3} \Rightarrow i_1 + i_2 + i_3 = 3$$

Rearranging the above matrix gives

$$0.2\begin{vmatrix} -i_1 \\ -i_2 \\ -i_3 \end{vmatrix} + \frac{1}{3} \times 0.2 \begin{vmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{vmatrix} . \begin{vmatrix} i_1 \\ i_2 \\ i_3 \end{vmatrix} + \begin{vmatrix} 0.95 \\ 1 \\ 1.05 \end{vmatrix} = \begin{vmatrix} 1 \\ 1 \\ 1 \end{vmatrix}$$

which, upon substitution of the KVL result, simplifies to

$$\begin{vmatrix} i_1 \\ i_2 \\ i_3 \end{vmatrix} = \begin{vmatrix} 0.75 \\ 1 \\ 1.25 \end{vmatrix} .pu$$

The simulation results for the differential droop scenario are shown in fig 4.6 and agree with the theoretical analysis. Note that, unlike the linear droop result, the voltage has not deviated from the nominal level.

4.3.2 Realistic Intermodule Communication Bandwidth

Fig 4.7 and fig 4.8 show the summarised results from the Simulink models of the developed load sharing methods. The two significant parameters in the sharing network are the differential droop coefficient and the communications delay. The three dimensional plots illustrate the effect that increasing the communications delay has on the systems transient and steady state load sharing and quality of response for a given differential droop coefficient. The simulink models have been normalised to a time base of $1rad/s$, i.e. the fundamental component of the reference waveform has a frequency of $1rad/s$. Initially the system has no plant load on the output. At $t = 8s$ a step increase to full load occurs.

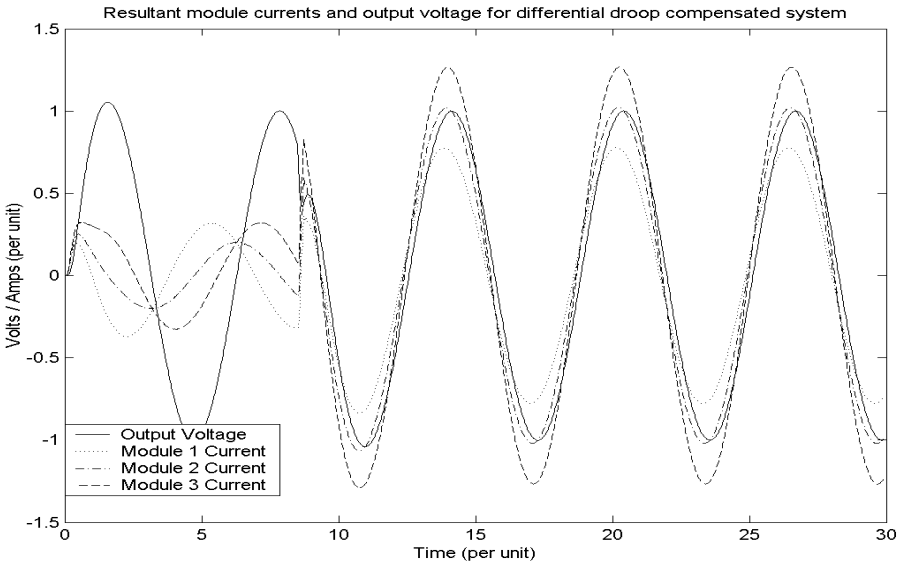


Figure 4.6 Results for differential droop compensated system : $G_{Droop} = 0.2$

The amplitude of the result indicates the level of imbalance between the modules. A small error between modules indicates good sharing, and typically occurs at low communications delays. A large error indicates poor sharing and probable instability.

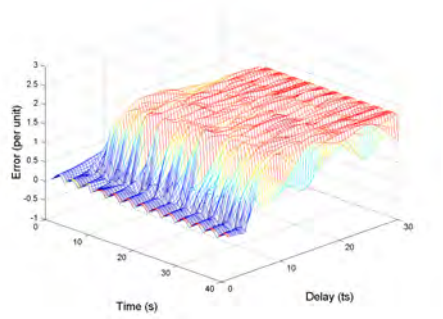
The figures in the right hand column are the output voltage deviation from nominal. The target error is zero, the error increases as the delay increases.

Figure 4.7 is for the slow local droop algorithm. In this algorithm, the local current term is sampled at the same rate as the global average current term is updated - a fact of significance only as the delay increases. This method results in a minimisation of the voltage distortion, as the sampled currents are always from the same time quantum, however it leads to a low bandwidth local droop action which can (and does in simulation) result in instability.

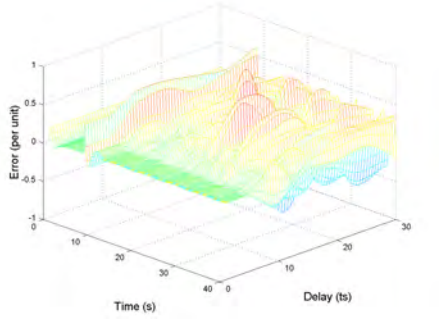
Figure 4.8 is for the fast local droop algorithm. In this algorithm the local current term is sampled at the sample rate of the local control loop, while the global current term may be updated at a considerably slower rate. This method results in a high bandwidth local droop action which results in a very stable system, however there will be an average phase error between the global current term and the local current measurement, which leads to voltage distortion.

The results show that the communication delay in the system is a key parameter, especially for the slow local droop algorithm which is unstable at all by the smallest communication delays, though at these small delays it displays exceptional voltage regulation. The fast local droop algorithm is stable at all delays, but likewise needs small delays to maintain a low voltage distortion. Both systems show a decrease in sharing error and an increase in output voltage distortion as the droop coefficient is increased, and also a decrease in overall stability with increasing droop coefficient.

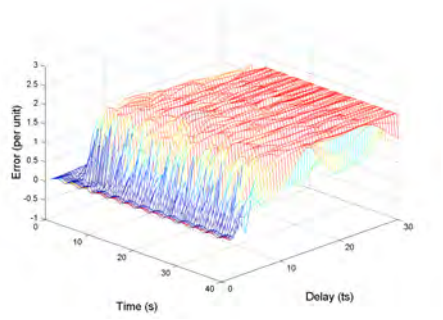
Of the two, the fast local droop algorithm seems more practical, though the relative merits are investigated in much more detail in chapter 6, this simulation result simply serves as an initial indicator.



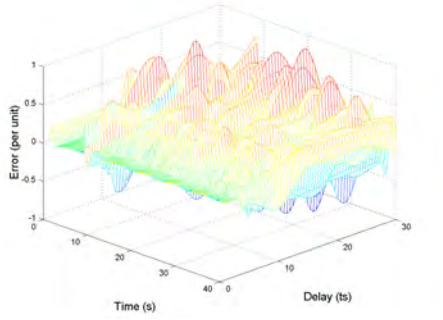
(a) Load Imbalance - Gdroop 0.2



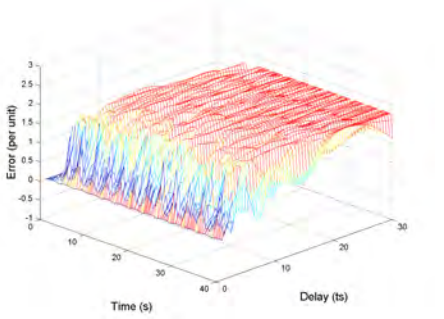
(b) Voltage Error - Gdroop 0.2



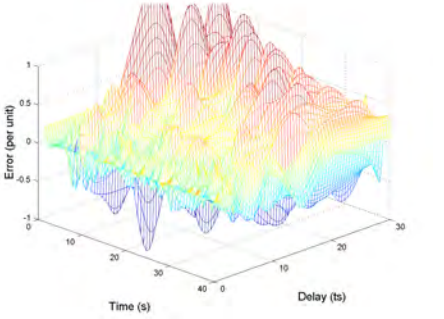
(c) Load Imbalance - Gdroop 0.5



(d) Voltage Error - Gdroop 0.5

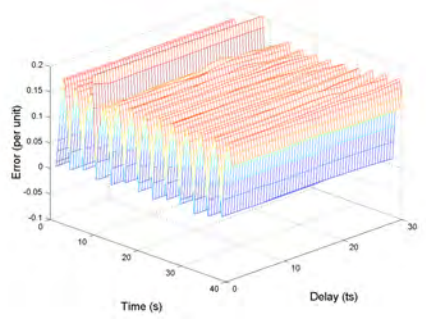


(e) Load Imbalance - Gdroop 1.0

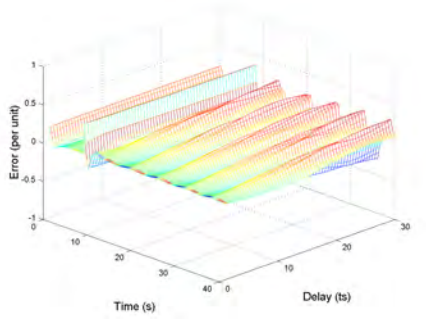


(f) Voltage Error - Gdroop 1.0

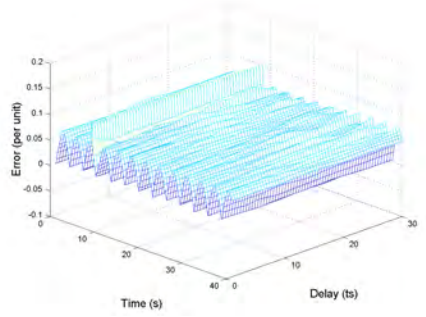
Figure 4.7 Simulated Result for Sample and Hold based sharing with delayed local droop feedback



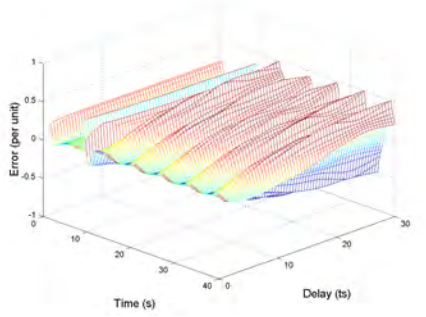
(a) Load Imbalance - Gdroop 0.2



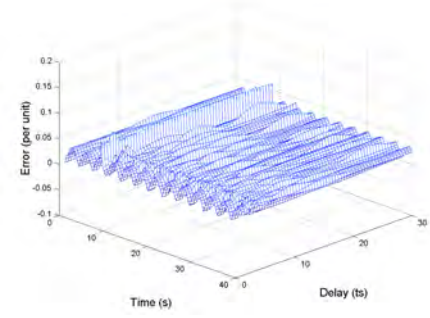
(b) Voltage Error - Gdroop 0.2



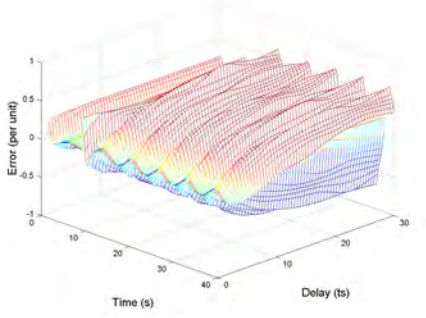
(c) Load Imbalance - Gdroop 0.5



(d) Voltage Error - Gdroop 0.5



(e) Load Imbalance - Gdroop 1.0



(f) Voltage Error - Gdroop 1.0

Figure 4.8 Simulated Result for Sample and Hold based sharing with fast local droop feedback

4.4 DC BUS OVER-VOLTAGE CONTROL

Among the problems involved with having multiple sources connected to a common bus is that circulating real power between sources can (in the case of a VSI) increase a modules DC bus voltage to the point that protection operates, taking the module offline. Without compensation this will occur even if the power flows in question are very small.

In VSI systems with an active rectifier front end the risk of this occurring is reduced, as the rectifier actively controls the DC buss voltage and is capable of bi-directional power flow. However, it is easy to imagine a scenario in which the inverter stage might re-enable before the rectifier stage, in which case no through path would exist and the DC buss would be vulnerable. An algorithm to regulate the buss voltage in the event of negative power flow is required. To achieve this the Magnitude of the inverter reference voltage phasor is made proportional to the DC bus voltage once the DC bus voltage exceeds a certain threshold illustrated in fig 4.9. A feedback gain of 0.5 was indicated as stable through simulation, as this function is independent of the number of modules within the system the experimental results gained from the proof of concept are complete evidence of functionality.

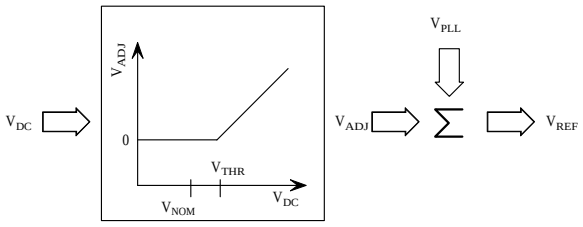


Figure 4.9 DC Bus Voltage Regulation Process

4.5 ALGORITHM PROOF OF CONCEPT

So far a number of theories regarding the effectiveness of actively paralleled systems have been proposed and investigated, both analytically and by simulation. Before developing a purpose built parallel system it would be prudent to prove the performance of the paralleling mechanism by experimentation.

This is accomplished using a 25kVA single phase module (VSPII Power Module) connected in parallel with a low impedance mains supply. The control routine locks onto the output phase and follows it to maintain synchronisation, essentially the system consists of one smart module actively balancing with the other dumb module (the mains).

These tests demonstrate the differential droop coefficients behaviour as a real impedance; the ability to avoid a DC bus overvoltage situation using the discussed control loop; and the effectiveness of differential droop with regard to stable current sharing between two current sources without degradation of output quality. The results are not completely indicative of a full system as the impedances are not matched, but the results remain relevant nevertheless. Discrepancies were observed and are explained in the following section.

4.5.1 System Testbed

The experimental setup is shown in figure 4.10.

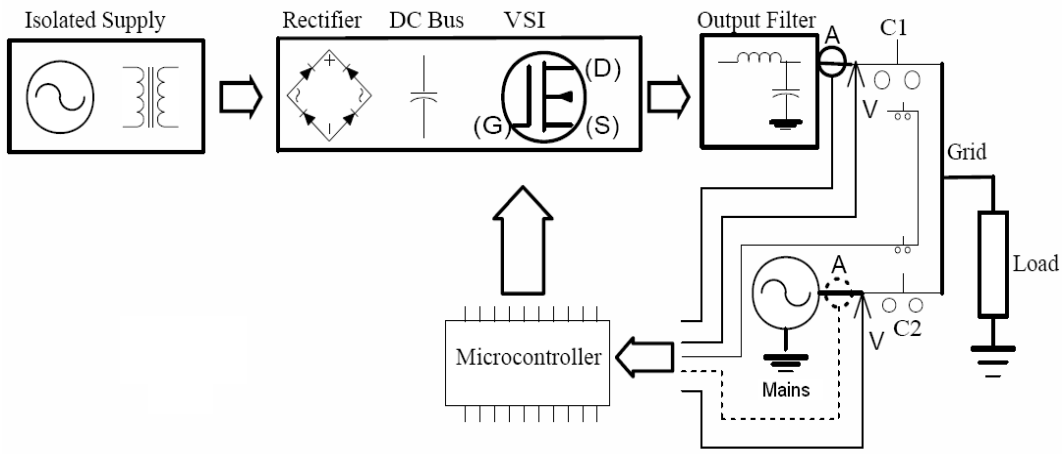


Figure 4.10 Inverter - Grid : System Layout

4.5.2 Synthetic Resistor Performance

In chapter 2 a number of methods of load balancing were identified. Active load balancing based on the adjustment of reference parameters using a differential droop system was identified as the method with the most promise. This method relies on the control systems ability to first zero the effective impedance of the inductor at the fundamental frequency by controlling the inductor current, and then introduce a resistive term (proportional gain) in the control loop to function as a synthetic impedance to allow sharing. This section tests the effective output impedance of the system following the addition of the synthetic resistor by adjusting the reference voltage phasor and measuring the resultant current flow.

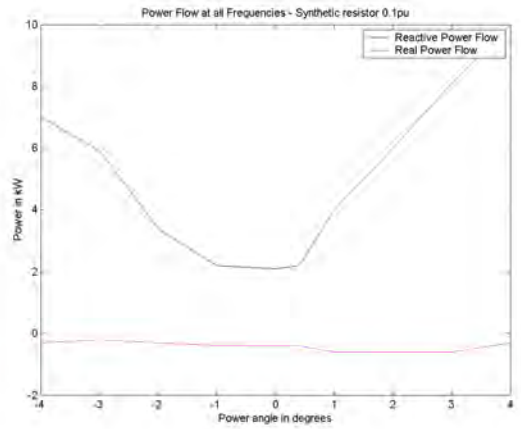
Power Flow in Response to an Angle Variation

Real power flow between active sources results from an angle difference for sources separated by purely complex impedance, and an amplitude difference in the case of a purely real impedance, as explained in Appendix A.1. The real and reactive power flows as a result of reference angle adjustment are given in figure 4.11. The power flows in fig 4.11(a) were taken directly from the readout of a Fluke39 power meter, and take power flows at all frequencies into account. These do not paint a promising picture, however the controller is only designed to accurately regulate power flow at the fundamental. Finding the real and reactive power flow proportional to power angle based on the fundamental current and phase angle gives the relationship shown in fig 4.11(b). The relationship between power angle and power flow is immediately apparent, and correlates exactly with what would be expected from a purely resistive impedance. This is strong supporting evidence, but it is also necessary to confirm the effect of a voltage amplitude change before the synthesized resistor can be declared effective.

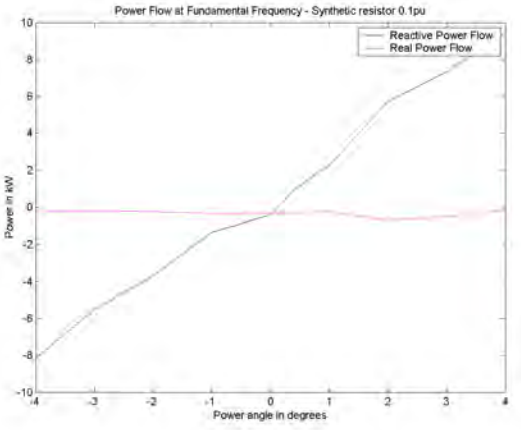
Power Flow in Response to an Amplitude Variation

An amplitude variation should result in real power flow through a resistor. Results from testing are shown in fig 4.12(a) for the full spectrum case, and in fig 4.12(b) for the fundamental.

There is a linear relationship between real power and voltage offset, while voltage offset and reactive power appear un-coupled. This, taken in conjunction with the results of the previous section, is sound evidence both that the synthetic resistor is acting as a real resistor for the purposes of fundamental current, and that the real inductor in the VSI output appears as a near zero impedance at frequencies within the bandwidth of the system. The clear limit on

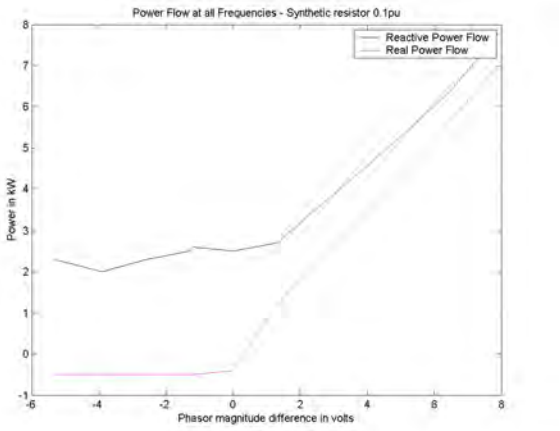


(a) All frequencies.

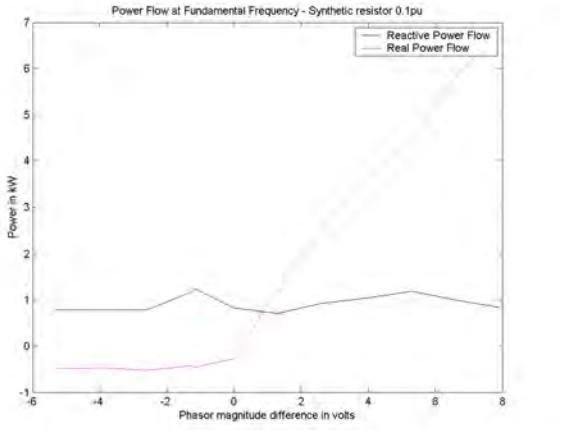


(b) Fundamental only.

Figure 4.11 The effect of the power angle on power flow in the system of Figure 22

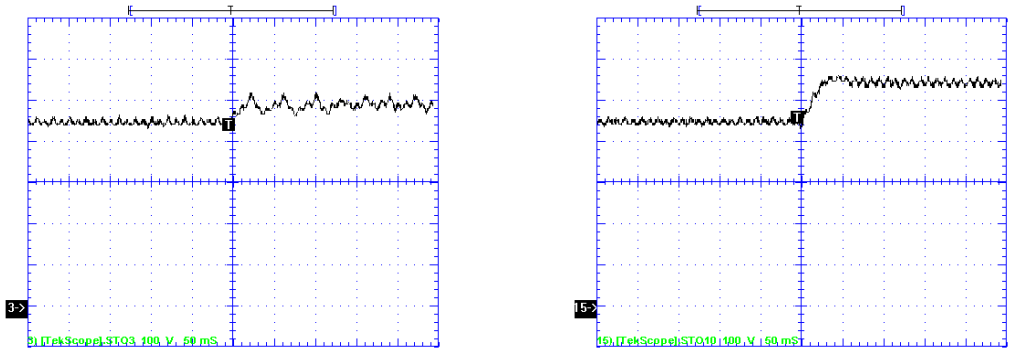


(a) All frequencies.



(b) Fundamental only.

Figure 4.12 The Effect of Amplitude on Power Flow in the system of Figure 22



(a) Feedback gain = 8.

(b) Feedback gain = 1.

Figure 4.13 DC Bus Voltage in Event of Negative Real Power Flow

negative real power flow is a result of the DC bus over-voltage prevention system described in the following section.

4.5.3 DC Buss Over-Voltage Control

The DC Buss overvoltage protection algorithm discussed earlier was implemented on the VSI controller and a deliberate phase offset introduced to cause negative power flow through the output inductor. Remembering the stability threshold was a gain of 0.5 by simulation, tests were conducted at a range of gains to determine the actual stability criteria after the influence of un-modelled damping elements. Results are shown in the referenced figures.

The damping within the system is evidently sufficient to stabilise it at gains much greater than those identified as allowable from simulation, though significant ringing on the DC bus voltage, as shown in fig 4.13(a), indicates the underdamped nature of the loop at high gains. Considering the likely voltage error and the allowable bus voltage envelope, there is little cost in using a conservative gain to ensure a stable response, as in fig 4.13(b).

4.5.4 Load Sharing Using Differential Droop

Having proved the operation of the synthetic resistor in the VSI control loop, we can use the resistor to allow balanced parallel operation with another source of near zero impedance using differential droop, as explained earlier in this chapter.

The VSI controller has a redundant current measurement channel which is easily configured to record the current flowing through the grid connection, making the information directly available to the controller with no need for the networked communication that will be required in the larger system. This is shown in fig 4.10 as measurement point A(C2).

There are two items of interest here. Firstly, will the differential droop algorithm prove to be stable in an physical system in an ideal case. Secondly, will it remain effective when the sample rate is lowered to a level similar to that likely to be achievable in the parallel network.

4.5.5 Steady State Response

Evaluating the systems performance is complicated by the presence of the harmonic circulating currents. To mitigate this issue, the system is run at a high load to increase the fundamental component. The harmonic in the voltage output is very small, so increasing the purely real load results in little additional harmonic current.

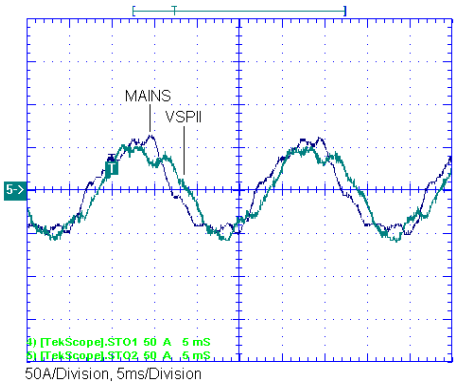


Figure 4.14 VSI and Mains Sharing : Steady State

The two waveforms shown in fig 4.14 illustrate the currents flowing from each of the two sources into 18kW of load. There is a significant load imbalance evident, however by inspection the fundamental component is fairly balanced. The circulating harmonics are due to the difference in output impedance with respect to the load. The circulating components would be much smaller in a balanced system of voltage sources as the impedances and voltage harmonic composition would match.

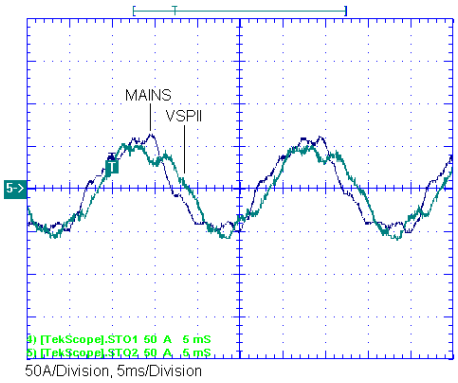
This result indicates the system is capable of operating in parallel with an source which has almost zero impedance, which is very promising as far as the parallel network is concerned. While this result proves the validity of the method, it is achieved at an unrealisable sampling rate using the existing communications structure. Decreasing the sampling rate has the effect of adding harmonic distortion and a phase delay to the 'averaged' reference. The results are shown in fig 4.15. The interval is in units of unmodified sample rate, 250μs for this controller. These results are similar to those given by simulation at the same sample intervals. This test is not a perfect analogy for the networked system, as in the ideal delay case the harmonic circulating current should not exist to the same extent in the networked system as the output impedances of the sources will be much more symmetrical. However, one of the attributes of the system is that it will allow effective sharing with asymmetries in impedance. The results of this experiment indicate this will be achievable with a sampling interval below 2.5ms. Between 2.5ms and 5ms circulating current becomes significant, and above 5ms it is well past acceptable limits. It is expected that a 2ms sample interval will be sustainable for brief periods in networks of up to ten modules in the event of a lost message packet.

Additionally, the absence of significant power flow at the fundamental constitutes proof of the differential droop action. The grid, as a low impedance source, will continue to produce nominal voltage regardless of the load. Power flow theory tells us that if the VSI were producing a different voltage over the small system impedance then we would observe significant circulating power at the fundamental. The absence of this circulating power flow therefore proves the differential droop action is operating as simulated and maintaining the system output voltage at the nominal level.

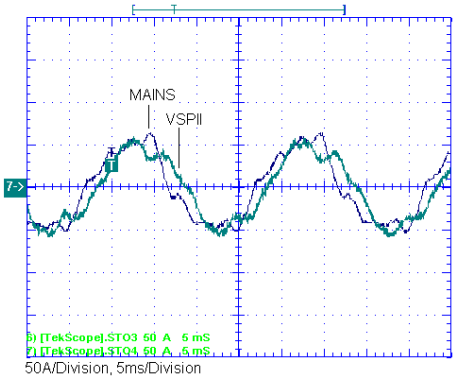
Based on these results, the load sharing method should be acceptable for steady state regulation. Now it needs to be tested for stability in response to a step load change.

4.5.6 Step Response

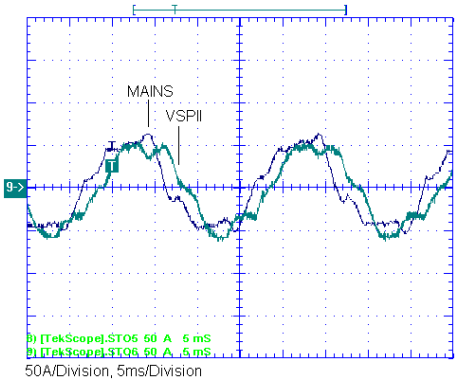
The step response shown results from a load being added to the already paralleled system. The key concerns are that the abrupt change will result in a significant circulating current, and/or that the impulse will excite unstable elements of the system. At the moment of switching there



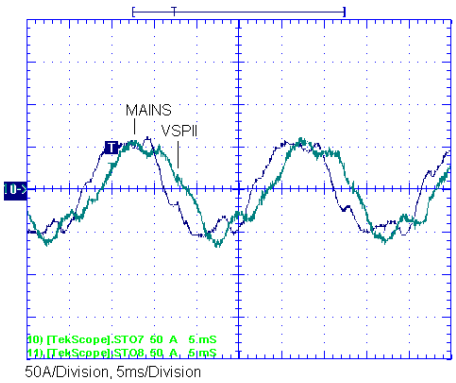
(a) Interval = 1.



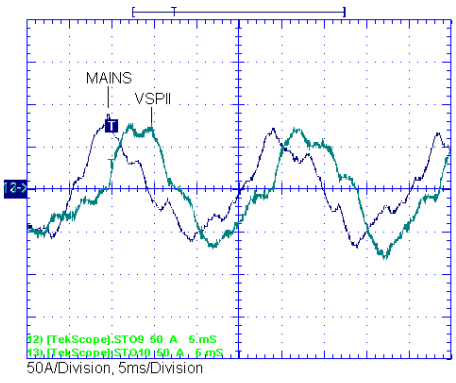
(b) Interval = 3.



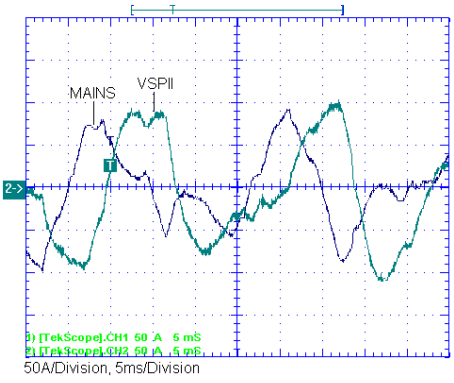
(c) Interval = 5.



(d) Interval = 10.



(e) Interval = 20.



(f) Interval = 30.

Figure 4.15 Steady State Current Sharing: Periodic Sampling.

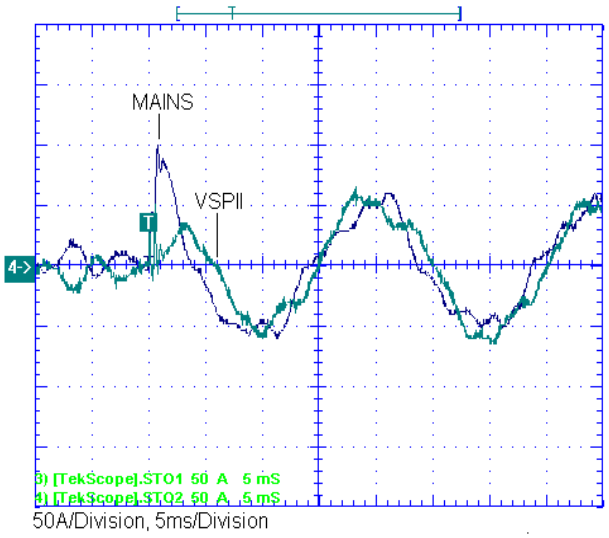


Figure 4.16 VSI and Mains Sharing : Step Load Change

is a momentary burst of current from the VSI output capacitor. This is evident in fig 4.16 at time $\approx$ 10ms. In the networked system this would lead to a collapse in output voltage which would elicit a more rapid response from the VSI, but in this case the voltage is maintained by the mains, which sources the majority of the load in the short term following the spike from the VSI output capacitor. Therefore the control loop doesn't receive any indication that the current needs increasing (as it would were there a significant voltage error) until the next current sample comes through and the imbalance between VSI and mains currents is identified. This delay is the cause for the significant error between time = 10ms $\rightarrow$ 15ms. The system appears stable, with the majority of the imbalance at low sampling intervals at non-mains frequency as a result of the impedance imbalance between the systems. This is expected and would be substantially reduced in a symmetric system. Fig 4.17 shows the effect of increasing the sample interval, large sample intervals lead to instability as shown in fig 4.17(f).

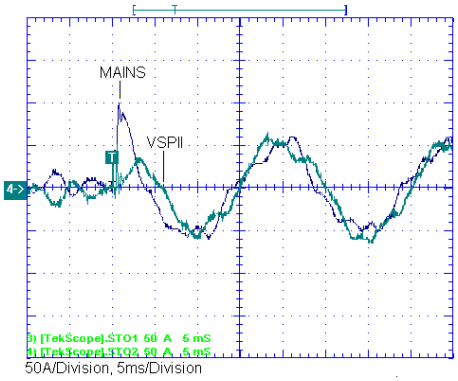
4.6 SUMMARY

Active control provides superior parallel performance to passive methods with regard to both load sharing and output regulation. A new load balancing mechanism termed 'Differential Droop' was developed in this chapter. It is the software equivalent of a lossless resistive impedance between modules that does not appear in the system output impedance, i.e. the impedance exists only for the circulating current. This is achieved by drooping the output reference based on the differential current component; the difference between the instantaneous module current and nominal module current. The algorithm is intended for implementation on a multiple master closely coupled system comprising semi-independent modules connected by a high speed communications link.

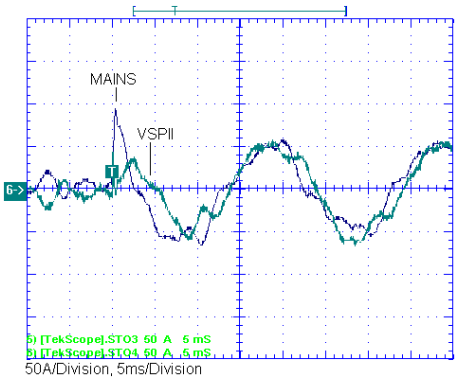
Two key limitations inherent to the method were identified; the communications delay and the quantisation of the sensed currents. Their likely effect was analysed and confirmed to be within the requirements of the design specification and also able to be mitigated by additional control elements.

Simulation of the system performance was completed for a representative 3-module system with an introduced error term. Both absolute and differential droop control methods were simulated to illustrate the benefits of differential droop. The results agreed exactly with theory.

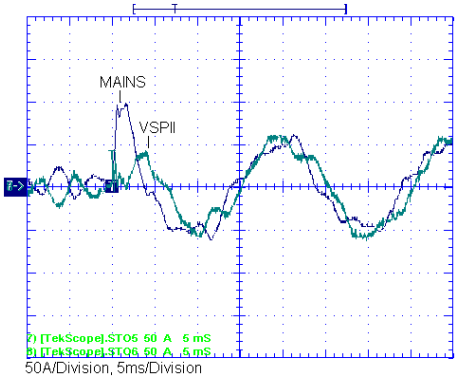
Further simulations were then conducted at communication data rates realistic to the topology



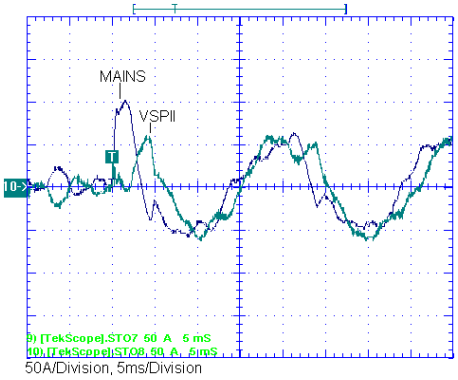
(a) Interval = 1.



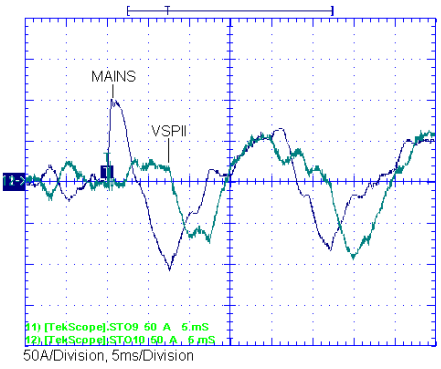
(b) Interval = 3.



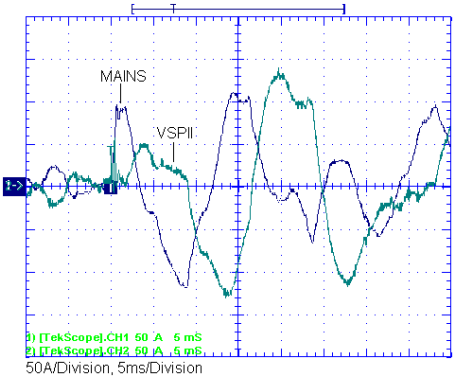
(c) Interval = 5.



(d) Interval = 10.



(e) Interval = 20.



(f) Interval = 30.

Figure 4.17 Step Load Current Sharing: Periodic Sampling.

to determine the system stability limits with respect to loop delay. As a result of this, a further development to the system was made with the introduction of fast local droop. This results in gradually increasing output distortion if the data rate drops, but ensures system stability is retained regardless of data rate. A further control algorithm was developed to prevent DC bus over-voltage events due to circulating real power.

A proof of concept system was assembled comprising a single module actively paralleling with a low impedance voltage source. A series of tests were conducted, proving the function of the synthetic impedance as a true lossless impedance, and then continuing to test the performance of the DC buss over-voltage protection algorithm and finally performance of the differential droop algorithm in both steady state and transient conditions. Performance at high data rates was excellent in all regards, but as the slow local droop algorithm was implemented performance at low data rates was unacceptable, as anticipated. This is not seen as a failure, quite the opposite in fact as it was congruent with the theoretical analysis and gave confidence that the system would operate as expected in a multiple module system. The next step is to develop software to allow the algorithm to be implemented in such a system.

Chapter 5

ACTIVE LOAD SHARING MULTI MODULE IMPLEMENTATION AND TESTING

5.1 INTRODUCTION

This chapter explains the software and hardware infrastructure developed to support the active paralleling algorithm developed and proven in the previous chapter. To begin with, the specific requirements of the algorithm are detailed based on the investigation and results of the previous chapter. The implementation of the mechanisms used to meet these requirements is explained, and test results of each element in isolation are presented to prove they perform as intended. An analysis of the performance of a two module system operating in parallel using the developed algorithm is presented in the following chapter.

5.2 CONCEPT

The control platform present in each module was developed with the intention that the modules would be paralleled. As such it has two key features simplifying synchronisation. The first is a CAN interface, allowing system wide sharing of variables. The second, and key to synchronisation, is a dedicated external interrupt line able to be both driven and monitored by all controllers in the system. The line drivers and characteristics offer low skew and high noise immunity. The receive element directly triggers a hardware interrupt on the controllers DSP and so provides very fast response.

The proposal is to use a combination of the CAN and the dedicated line to align the reference waveform zero crossings. The precision of the processors local clock is expected to be more than sufficient to ensure the waveforms remain synchronised during the period between zero crossings, this will be confirmed in testing. While the communication networks have high error immunity, the system should be error tolerant, and also continue to function correctly in the event that modules drop offline through either user intervention or fault.

The CAN will also be used to distribute the instantaneous module currents, allowing each module to determine the average module current, calculate the differential current term, and droop their output accordingly.

The load sharing process will also embody the system configuration management, allowing tracking of the number of modules within the system and any other relevant information.

The system topology suggested, which is also the hardware setup used for the algorithm testing in this and the subsequent chapter is shown in figure 5.1.

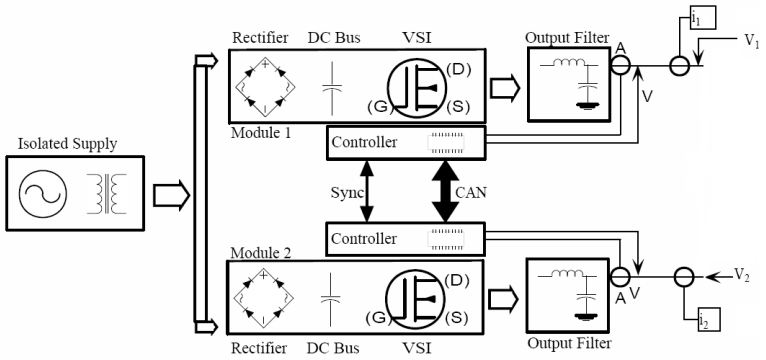


Figure 5.1 System Topology

5.3 AVAILABLE INTERMODULE COMMUNICATIONS CHANNELS

Before discussing the methods used, a brief summary of the communication channels available is valuable to provide an insight into the constraints within which the design must exist. At present the control platform intended for the parallel system has two dedicated intermodule communication channels as follow:

5.3.1 CAN Network

The CAN network is a bi-directional differentially driven, optically isolated, twisted pair operating 5V logic and controlled by the DSP. It is specified to be extremely noise resistant and very unlikely to allow undetected communication errors. The maximum data rate is 1Mbit/s.

5.3.2 External Interrupt Line

The external interrupt line uses the same isolation and differentially driven 5V line as the CAN network. The line is driven by one of the general purpose ports on the controller, and monitored by the dedicated external interrupt line XINT1. Using this medium, any controller on the network can trigger an interrupt service routine simultaneously on all controller's, itself included. In addition to this, each controller has a 16 bit up-counter associated with the XINT1 line. While enabled, this counts upwards continuously at the controller clock rate rate, wrapping around when it reaches 65535, and is reset to zero when a valid interrupt edge is detected. This allows precise measurement of the time since the interrupt occurred.

5.4 ALGORITHM REQUIREMENTS

This sections outlines the features required to allow the differential droop algorithm to function as intended. These have been selected based on examination to identify key components of the control loop and matlab models used for the theoretical analysis.

5.4.1 Synchronisation of Reference Waveforms

Early stages of theoretical analysis and simulation showed conclusively that closely synchronised control reference waveforms were crucial in a system employing distributed control. A phase or amplitude error in reference waveform between modules will obviously cause a differential voltage, which will lead to circulating real and imaginary current between modules. While the paralleling mechanism will still act to correct the imbalance, the system performance will

be substantially improved if the open loop error is minimised. Synchronisation is an absolute requirement even without the requirement for low circulating power flow, as without it long term clock drifts within local waveform generators would completely corrupt the output of interconnected systems.

The proof of concept model used a phase locked loop to align its local reference to the mains waveform. While it would be possible to use a similar mechanism in this algorithm, with all modules phase locking to a designated master modules output, doing so would introduce a significant lag into the control loop with detrimental consequences for system stability and bandwidth. Additionally, the master module would not have the low source impedance of the grid in the proof of concept case, which would further compromise performance. A feed forward system is preferable as it allows higher precision, extremely fast transient response, and if implemented carefully can avoid the single master dependency of the previously described system.

5.4.2 Instantaneous Global Current

In order to implement differential rather than absolute droop it was shown that each local control loop required access to an instantaneous global current variable. Likewise, the instantaneous local current is also required, however this is already a standard feature of the voltage control algorithm used and does not need to be considered as an addition to a parallel system.

The proof of concept system directly measured the currents in each parallel element in the system to arrive at a value for the global current, a method that is totally impractical for application to large distributed systems. An alternative based on the communications network is proposed for this topology.

5.4.3 Differential Droop Added to Existing Control Loop

The differential load based correction term must be added to the already developed control loop in such a way as not to compromise system integrity and stability anymore than expected from simulation. The correction term must be accurate in consideration of the number of modules within the system and the per unit rating of each module. This was implemented in the proof of concept system of chapter 5 without issue, however the control algorithm and control platform use in the proof of concept were of the generation prior to those on which this prototype is to be based, so the modification must be repeated and revalidated.

5.4.4 System Management and Redundancy

The paralleled system must be able to keep adequate track of its constituent elements to ensure the nominal system rating (and hence individual module responsibility for load) remains accurate, synchronisation of the reference waveforms and scheduling of current variable sharing actions occur in a timely manner, and module failures are recognisable and redundant operation possible. Redundant operation requires that the modules are able to locally isolate themselves from the supply and output, while this problem is complimentary to the goals of this development it is also outside the scope.

5.5 SYNCHRONISATION OF REFERENCE WAVEFORM

The aim of the reference waveform synchronisation is to reduce error between control loop references to the minimum possible level. The minimum standard of acceptance for the load sharing algorithm is a circulating current of 0.05 per unit, which equates to a maximum differential

voltage at the fundamental of 0.01 per unit at a droop of 0.2. This also fails to take into account all other possible sources of circulating current (the most significant of which is the voltage feedback sensing error), so the error in open loop waveform generation after synchronisation will need to be substantially less than this.

5.5.1 Method

To accurately generate a reference waveform of the form

$$v(t) = Asin(\omega t + \theta)$$

it is necessary to know the amplitude (A), the frequency (ω), and the phase offset (θ). The amplitude and frequency are published onto the system communications network as they're adjusted, and applied locally by the waveform generator of each module. All that remains is to remove and phase difference between module references. The 'sync line', performs the primary synchronising action. The reference waveform is generated by a continuously wrapping variable representing θ_{ref} being used to index a sine table, with θ_{ref} being incremented at such a rate as to give the desired frequency. The wrapping nature of theta gives an easily measurable periodic event, the $2\pi \rightarrow 0$ transition. The first module to register a wrap occurring drives the sync line high, triggering an interrupt service routine in all controllers on the network. This interrupt service routine sets a flag, which causes the control loop to transition to a 'sync ready' mode in which all modules continue normal operation, but additionally listen for updated synchronisation data to allow accurate synchronisation in consideration of the following two potential sources of error. Once all data is available, the reference angle is updated according to equation 5.1.

Skew Compensation

While it would be simple to zero the angle reference as a response to a synchronising interrupt, this would not produce an ideal result. Because the sampling and switching is asynchronous between modules, there could be as much as one sampling period of phase difference between modules. In the case of a system operating at a $50\mu s$ sampling rate and a fundamental frequency of 50 Hz this results in a phase error of 0.25%, giving an RMS voltage error of 1.5%, which in turn would give an RMS current error of 7.5% using a $0.2p.u$ synthetic resistance. Given the tolerances required of the final solution this is a significant error, so some method of correcting for the distortion is needed.
The solution comes with the external interrupts 16 bit counter. This has a resolution of one system clock cycle, which is far more than required to accurately record the amount of skew. When the interrupt is asserted, the clock is reset and begins counting up, keeping a record of the elapsed time which permits compensation.

Quantisation Compensation

Using the above process the waveform can be synchronised accurately between multiple modules. However, the zeroing of the waveform reference once a period can cause a jump in the waveform. The sine table referencing is implemented as a continuously wrapping process, the exact values given depend on the ratio of waveform period to the period of a control loop sample-process-wait call. The result of waveform period over control loop repetition period will likely be a non-integer, with the result that the sine table will be indexed at different points each time it is cycled through. Zero will only occasionally be one of these points. If the waveform is reset to zero every time a synchronising process occurs, a phase jump equal to the actual angle reference at the moment of synchronisation will occur. To avoid this a way of synchronising the waveforms

to a common reference while retaining the wrapping action is required.
This is achieved by using the angle of the self appointed master unit at the moment the synchronising interrupt occurs as the reference to be synchronised to, instead of using zero. As this reference will not be a constant value, the slave modules must have access to it on a cycle by cycle basis. To facilitate this, the reference is broadcast by the master over the CAN network as part of the synchronising action. When the variable is received by the slave modules they synchronise to it using the 16 bit interrupt counter to compensate for the transmission delay as illustrated in fig 5.2, step 4. The equation used to realign the waveforms is given below.

$$\theta_{ref} = \theta_{sent} + \theta_{calc} \tag{5.1}$$

where θ_{sent} is the value sent out over the communications net, and θ_{calc} is determined locally using the interrupt triggered clock as below

$$\theta_{calc} = \frac{t_{elapsed}}{f_{clock}}\omega \tag{5.2}$$

f_{clock} is the interrupt triggered clocks frequency in counts/second, $t_{elapsed}$ is the integer count held by the clock at the moment of θ_{calc} calculation, and ω is the systems fundamental frequency reference in radians/second.

Sub-cyclic Reference Drift

The entire reason for the synchronisation process is that waveforms are expected to drift apart over time. As this drift will be a continuous process, some finite drift will occur in the space of one cycle despite close synchronisation, and to bring the waveforms back into line some further distortion is inevitable. While it would be possible to change the reference frequency very slightly to gradually slew the waveforms back into alignment, that level of complexity is probably unnecessary given the clock accuracy and resulting very small errors. The accuracy of the system clock is given as one part in 30,000, so the maximum potential phase jump at $50Hz$ as a result of clock drift is around 0.0033%, a completely insignificant amount. The distortion resulting from realigning the waveforms over the space of a single sample period will not be an issue.

Graphical Representation

The graphical representation of Fig 5.2 illustrates the synchronisation process described in this section, including the skew and quantization compensation. The diagram is not to scale, in reality the entire process occurs within the first $250\mu s$, or approximately $\frac{1}{80}$ cycle at 50Hz. The sequence is described below, the numbered steps corresponding to the numbers in the figure.

1. The reference waveform for module 1 wraps around.
2. Module 1 executes a high speed control interrupt service routine (ISR), recognises the wrap around has occured, asserts the sync line momentarily to indicate its role as master, and begins transmission of the θ_{sent}.
3. A control ISR occurs on module 2, it likewise realizes a wraparound has occured but also recognises that another module has already begun the synchronisation process, as indicated by the momentary assert on the sync line. As such it continues as normal, awaiting the arrival of θ_{sent} before realigning its reference.
4. Another ISR occurs on module 2, it now realises that θ_{sent} has arrived and realigns its reference as described in equation 5.2, leading to the step in the waveform 2.

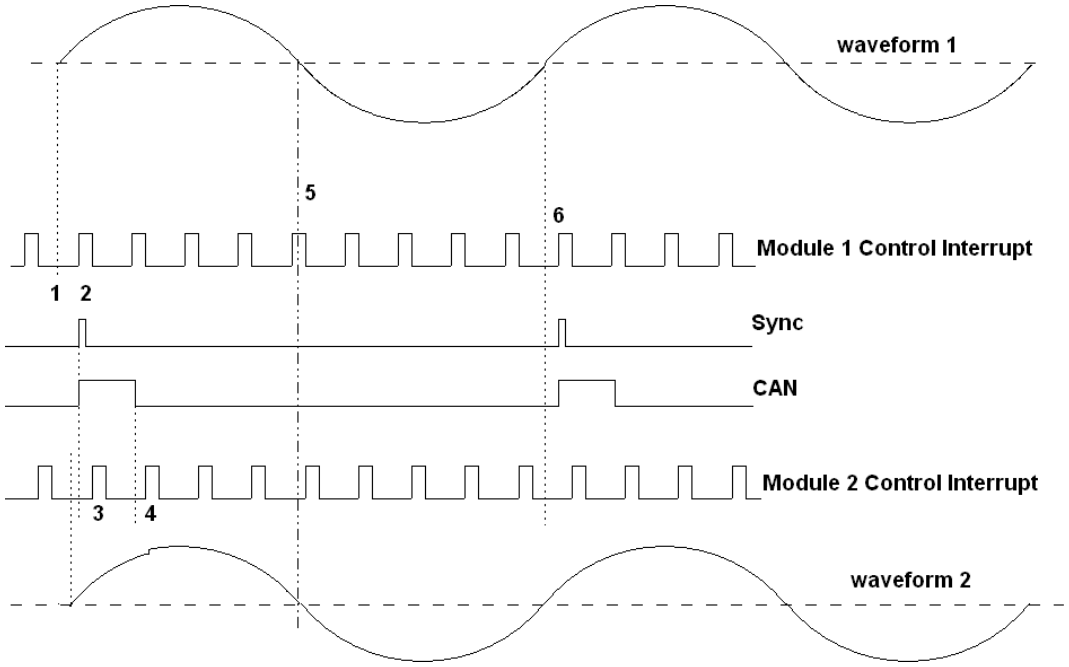


Figure 5.2 Graphical Representation of Synchronisation Process

5. Both waveforms are now synchronised.

6. Another zero crossing occurs, and the process repeats.

5.5.2 Results

This section tests the controllers ability to synchronise the reference waveforms of two independent modules. The synchronisation routine must comply with three requirements as follow

1. Synchronisation of output to accuracy sufficient to produce near zero circulating current.

2. Resynchronisation in event of temporary CAN failure.

3. Resynchronisation in event of temporary Sync line failure.

This section demonstrates that the synchronisation process can align the reference waveforms of multiple modules to a very high precision. The error will decrease further still once the switching carrier waveforms are also synchronised. The synchronisation routine is fault tolerant, and waveforms have an extremely low rate of diversion in the case of transition to isolated operation as a result of an error.
The synchronisation algorithm was tested by following the sequence described below -

1. Both communication lines active.

2. Both communication lines disabled and held disabled for 120 seconds.

3. Both lines re-enabled.

Two measurements were made for each of the operating conditions listed, namely -

1. Line to ground voltage waveform of each module with Oscilloscope.

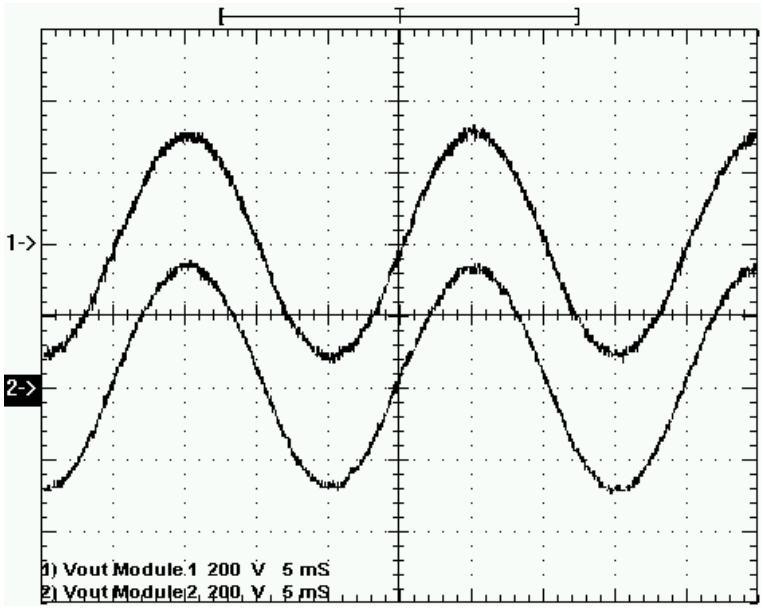


Figure 5.3 Synchronised Module Output Voltages

2. Line to Line differential voltage between synchronised common neutral referenced outputs with harmonic voltage meter.

The test setup used to obtain is that shown in fig 5.1 at the beginning of this chapter. For this test the only connections between the two inverter modules were the CAN and Sync lines, and a common neutral line at the output to enable direct measurement of the differential output voltage. Excluding the effect of the synchronisation algorithm, both inverters are running the unmodified closed loop control algorithm described in Appendix C. The variable of interest in this experiment is the differential voltage between the inverters outputs. If the synchronisation algorithm were perfect the differential voltage would be near-zero, the only error source being minor variations due to the inverter power stage and feedback sensing inaccuracies.

Intermodule Error While Synchronised

This test was performed with both modules enabled and running, both communication lines fault free, and both contactors open. By observation the output waveforms were near indistinguishable, as shown in fig 5.3. To gauge the error more accurately one terminal of each module was connected and the voltage between the two unconnected terminals was measured using a Fluke 41 meter to identify the harmonic components. The bar plot in figure 5.4 shows the results.

The total differential voltage is approximately 2%. For load error calculation this can be taken as one module operating at 1% above nominal, and the other 1% below nominal. This would lead to a load error of $\pm 5\%$ respectively with the intended $0.2p.u$ synthetic resistor, which is significantly more than the target value. However, inspection of the harmonic makeup of the voltage error term indicates that the majority of the error arises from the DC voltage term, which should be mitigated by more accurate tuning of the gain and offset coefficients for the voltage transducers, and the harmonic terms which are a result of the unsynchronised PWM carrier waveforms. An alternative method for reducing the DC voltage error is to highpass filter the feedback voltage to run the DC voltage generation in pure open loop. DC voltage error from waveform generation and the power stage should be minimal, and the resulting circulating current flow will be managed by the intrinsic cancellation due to deadtime described in chapter

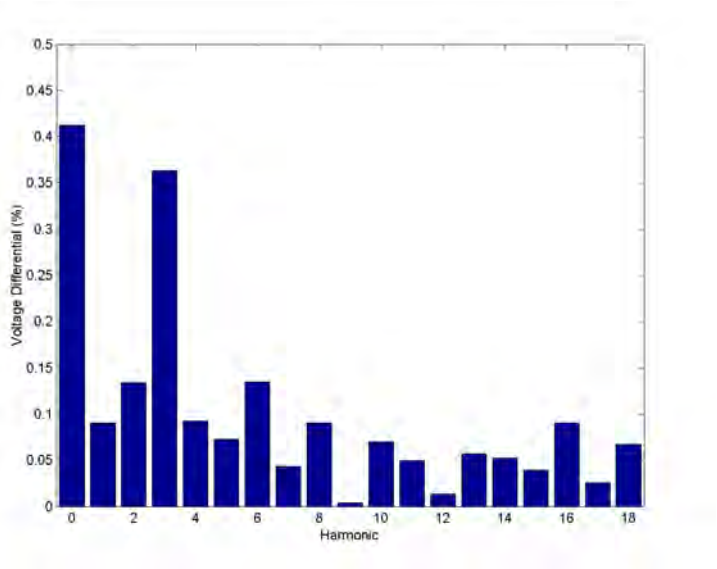


Figure 5.4 Differential Voltage between Synchronised Modules

3. The fundamental voltage error is less than 0.1%, which indicates modules are within ±0.05% of nominal. This means that the fundamental load error could be expected to be less than ±0.25% of full load current, which is exceptionally good.

Based on this result, if the PWM carrier waveforms are synchronised using a similar method to that used for reference waveform synchronisation, very small differential voltages should be achievable.

Resynchronisation in event of temporary CAN failure

A CAN failure was simulated by shorting the differential communication lines together. This will result in zero data throughput and errors generated by the CAN data handling routine. The lack of synchronisation leads to an increasing error between modules. The differential voltage after two minutes is shown in figure 5.5. The rate of drift when the modules are operating in isolation is very low, however the error is now observable and were the two modules connected under these conditions there would be significant circulating current despite the the synthetic resistor. The system immediately resynchronises the outputs to the accuracy demonstrated in figure 5.4 upon removal of the CAN fault.

This illustrates two things. The first is that the rate of drift between modules is sufficiently low that even if several synchronisation attempts were to fail in succession, no discernable error would result. The second is that the system is fault tolerant, returning to normal operation without the need for a reset process or similar.
Additionally, this test confirms that the developed synchronisation routine is the mechanism responsible for the small differential voltage error as opposed merely operating alongside some poorly understood additional beneficial feature.

Resynchronisation in Event of Temporary Sync Line Failure

The Sync Line uses the same driver as the CAN line, and a failure is simulated in the same manner. The CAN and Sync Line work together to synchronise modules, so it comes as no surprise that the result of the Sync Line fault is the same outcome as that of a CAN fault. Removal of the Sync Line fault results in the same immediate resynchronisation as when the CAN fault is

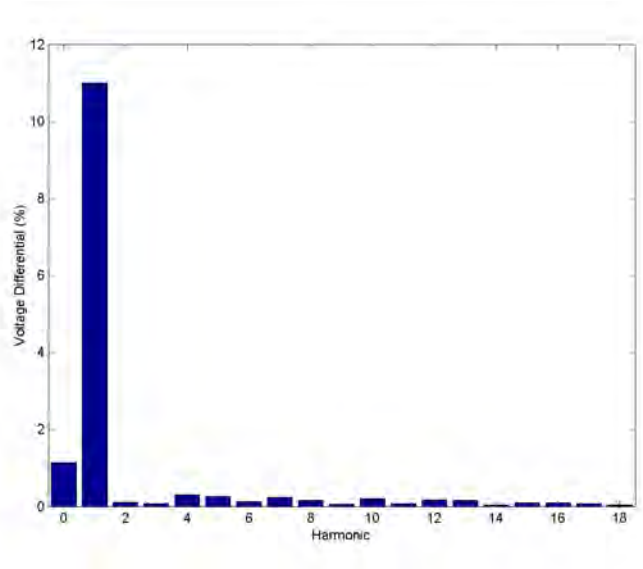


Figure 5.5 Differential Voltage Between Modules after 120s with no Synchronisation

removed.

5.6 DISTRIBUTION AND COLLATION OF INSTANTANEOUS CURRENT

This process must give each module the ability to determine the instantaneous average module current. It must be accurate enough to enable load balancing to within the required tolerance, which is actually not an issue considering all modules will deviate to the same extent in the event of an error. The real motivation for accuracy is that the comparison of the global current with local currents is what allows us to share without distortion of the output. An error in the global current will manifest as a voltage error. Our tolerance for voltage error is ±1%, which means the instantaneous global current must be accurate to within ±5%.

5.6.1 Method

There are two methods of determining the system current. The first is to measure it directly at the system output. This is relatively simple, but also reduces the modularity of the system as the CT will have to be sized to the system, and increases the cost as an additional CT will be required as well as supporting communications infrastructure.

Instead, the chosen method involves the synchronous sampling of the current by every module in the system, system-wide sharing of all sampled currents, and calculation within each module of the system current based on the locally measured and remotely transmitted module currents.

Key features are:

1. The skew between samples must be very small or else an apparent error will result proportional to $\frac{di}{dt} \times t_{skew}$.

2. The distribution of all currents must occur in a time period less than the maximum allowable delay identified in simulation.

3. The results must be globally available within the system.

4. The messages sent by each module detailing their local load conditions must be interpreted by each controller in such a way as to provide all information necessary to allow simple system management and module tracking.

Synchronous Sampling

As the system already has a synchronous and periodic variable, θ, the sampling of the current for the system current calculation was scheduled using this variable. The sample rate was determined based on the available CAN bandwidth and number of modules within the system, these two variables in conjunction with necessary data packet size determining the time per distribution event. The samples were then scheduled to occur at intervals of theta as shown below:

$$\frac{\mu s}{cycle} = \frac{1}{freq} \times 10^6 = 20,000@50Hz \tag{5.3}$$

$$\frac{\mu s}{share} = \frac{modules \times data}{dataRate} = 96 \times modules \tag{5.4}$$

$$\frac{Shares}{Cycle} = \frac{share}{\mu s} \times \frac{\mu s}{cycle} = 41.7(@50Hz, 5Modules) \tag{5.5}$$

$$\theta_{interval} = \frac{2\pi}{Shares/Cycle} = 0.151rad \tag{5.6}$$

The first sample always occurs with the synchronisation pulse to ensure no skew develops between samples over time. Subsequent samples for the remainder of the cycle occur every $\theta_{interval}rad$ after that.

Communication

The communication of all the data was simple using the existing CAN systems, and occurred as follows:

1. A sample is scheduled, each module measures the local current variable and loads the result into an outgoing message mailbox in the CAN manager and sets the associated transmit flag. The CAN layer deals with all transmission scheduling and retries.

2. Each module sits and waits for a receive interrupt event, and when it occurs retrieves the new value from the nominated receive mailbox.

Each message is sent in one → many format.

Collation and calculation

The collation is really a continuation of the communication process. As each value is read out of the receive mailbox, it is loaded into an array, and an integer representing the number of modules on the system is incremented by one. As each module only sends one message per interval, counting the updates gives the number of modules in the system. If a module fails for any reason, it no longer issues an updated current value, which means all the other modules will know there is one less module in the system and de-rate the system appropriately.

The total number of modules in the system is determined by the number of responses received in the space between two scheduled sample events. Clearly there will be a lag of one sample event for the system to update the number of modules following a change. The sharing mechanism operates regardless of the mode of the system, so it is reasonable to assume that there will be

time during startup to determine the number of modules before the system transitions to a run mode.

This mechanism is totally dependent on the module count being sufficiently small to ensure all updates are successfully communicated within the available time, and as such is not hugely robust. The process is as follows:

1. Module count set to zero, first value retrieved from incoming mailbox and added to system current array, module count incremented.

2. Process repeated for x modules

3. Final value retrieved from incoming mailbox. Module count incremented.

4. All values in system current array added together, and divided by module count to give average instantaneous current per module.

5. Resulting average loaded into appropriate control parameter.

6. Module count compared to module count from previous cycle to check for loss of modules and warning issued if necessary.

5.6.2 Results

The true test of the above mechanism occurs in the following section on control loop modification, as it is designed to operate in conjunction with the differential droop term, however a quick test of the algorithm was conducted by disabling the control loop output to the pwm counter (while retaining all waveform synchronisation as necessary for synchronous sampling) and instead outputting a fixed duty cycle m;
Modulation index m = 0.75 for module 1.
Modulation index m = 0.25 for module 2.
Both modules were running into independent linear loads, sized to the system so as to give 10A current at full modulation depth. The internal variables of each module were checked using a device emulator to read them directly from the DSP memory. Operation was confirmed with the communications bus active, and then again with it disabled, simulating the mutual loss of modules. The results are shown in fig 5.6.

The collation and calculation mechanism is functioning as intended and the correct system current is calculated. This is a not a particularly arduous test, as the DC nature of the current means skew in sampling time will not assert itself, however this will appear in the control loop test if present, and the good performance of the rest of the process is a positive sign.

5.7 CONTROL LOOP MODIFICATION

5.7.1 Aim

The modification to the control loop must modify the reference voltage to improve module load sharing based on the difference between the average current and the local module current. The control loop must not be destabilised, and no errors other than those already addressed are acceptable.

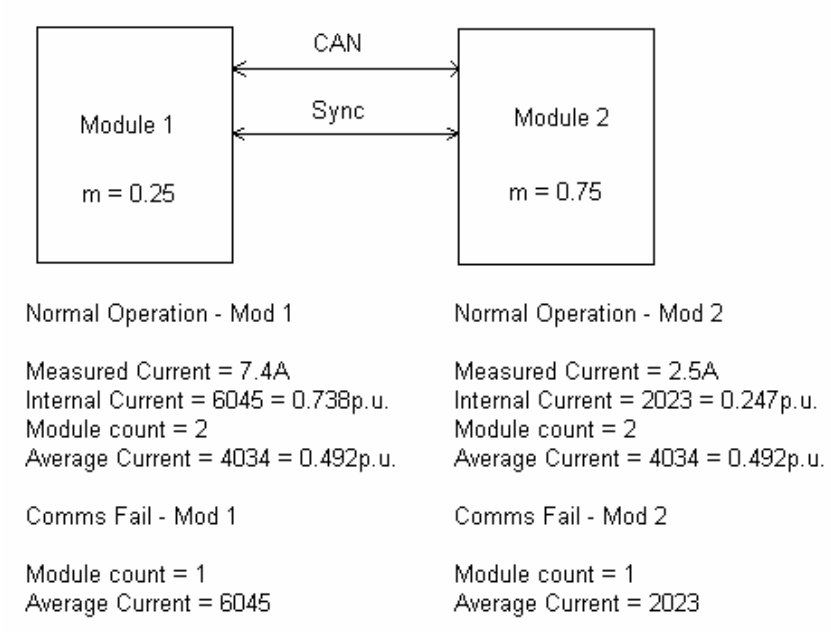


Figure 5.6 System current collation test

Figure 5.7 First Stage of Existing Voltage Control Loop

5.7.2 Method

This was easily implemented within the existing control loop as illustrated in the two diagrams, fig 5.7 and 5.8. Calculation times on a 150Mip processor are negligible in the context of an $8kHz$ sample rate.

5.7.3 Results

These results also prove the correct function of the instantaneous current distribution and collation mechanism in a transient environment.
As in the previous test case, two modules with different reference variables were used, though in this case the entire control loop was still linked up including the modified differential droop injection stage. The difference in variable was created by removing the link between the reference waveform amplitude and the communications network, and hard coding the amplitude variable to:
Module 1 Reference Amplitude = 1 p.u.
Module 2 Reference Amplitude = 0.5 p.u.
1p.u voltage= $231V_{RMS}$
1p.u current= $5A_{RMS}$
Obviously these reference voltage errors are hugely outside the system tolerances, this level of error is introduced to make the result more obvious. The two modules are once again connected

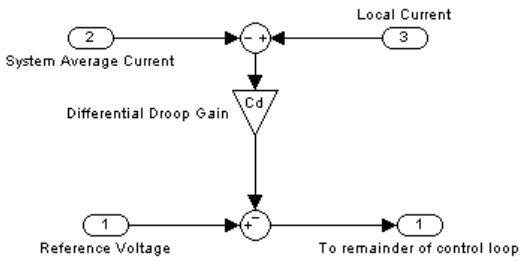


Figure 5.8 First Stage of Differential Droop Modified Control Loop

to independent 1p.u. loads. If the control loop modification is working, then it should act on the voltage term to reduce the difference in load between the two modules. If successful, this will appear as a change in output voltage on each of the modules. Initially the modules are run without the droop term set to zero to provide a basis for comparison. The results are as follow:

$C_{dr} = 0$

Module 1: $230V_{RMS}, 5.0A_{RMS}$
Module 2: $116V_{RMS}, 2.5A_{RMS}$

This is exactly as expected, the very small variations from the ideal are no different to what would normally be encountered.

$C_{dr} = 0.2$

Module 1: $221V_{RMS}, 4.8A_{RMS}$
Module 2: $126V_{RMS}, 2.7A_{RMS}$

This is the hoped for result. In recognition of its higher current, module 1 has decreased its RMS voltage, while module 2 at a below average current has increased its system voltage. Were the modules outputs connected to a common load, this action would directly reduce the load imbalance between the two modules. It bears repetition that this algorithm is intended to equalise the load between two already closely synchronised supplies, so the remaining large discrepancy between the currents in this case is no cause for concern.

5.8 SUMMARY

The reference waveform synchronisation and differential droop algorithm was implemented within the existing control framework by the addition of intermodule synchronisation and load sharing, and a modification of the local control loop.

In its present incarnation the system operates on a rotating master basis. One particular controller will take the lead role for a given synchronisation process, but the identity of this module is not specified in advance and were it to fail another module would take over the leading role without a reduction in quality of response or the necessity for an error message.

Testing of each key element in isolation was conducted, and the results indicate that the required performance has been achieved. Testing of all elements in an independent output system demonstrated a voltage control loop response consistent with the differential droop simulations

and provides a sound basis for testing of a coupled output system at low power levels in the following chapter.

Chapter 6

PROTOTYPE PERFORMANCE VERIFICATION

6.1 INTRODUCTION

In chapter 4 a method of balancing load between multiple VSI modules was developed and tested by simulation and on a proof of concept prototype. Chapter 5 identified issues associated with the real world implementation of this system and described the development of software to overcome these problems and implement the load sharing methods simulated. The function of the control elements in isolation was proven. This chapter reports on the performance of the developed system when applied to a real VSI multiple module network. Hardware availability constraints limited the number of modules to two, each module derated to $1.2kVA$. Though much lower than the target size, this is perfectly acceptable to prove the function of the synchronisation, sharing, and paralleling mechanisms.

6.2 TEST SETUP

The configuration described in this section was designed to prove operation of all the necessary control elements for a parallel system. The key requirements were as follows

1. An independent, though not isolated DC Bus on each module.

2. No external additional output resistance other than parasitic resistances within the conductors.

3. No connections between modules except for the CAN line, the Sync line, and the common output bus. The ac inputs to the rectifier stage are also common.

One necessary modification to the system that was not apparent from simulation was the insertion of common mode chokes in the output of each module. The reasons for this addition are outlined in the subsection on common mode current.

6.2.1 System Properties

The modules consist of an uncontrolled full wave diode rectifier front end, feeding into a high voltage capacitor bank of $100mF$ in one module and $160mF$ in the other. The output is an H bridge configuration of IGBT's. The original rating of each power module was 100A, however for these tests they have been derated to 5A. The output filter consisting of a $730\mu H$ inductor and $3\mu F$ capacitor is appropriate for this reduced rating. A 300W load was used to prove operation, this was increased to 2.4kW for collection of results.

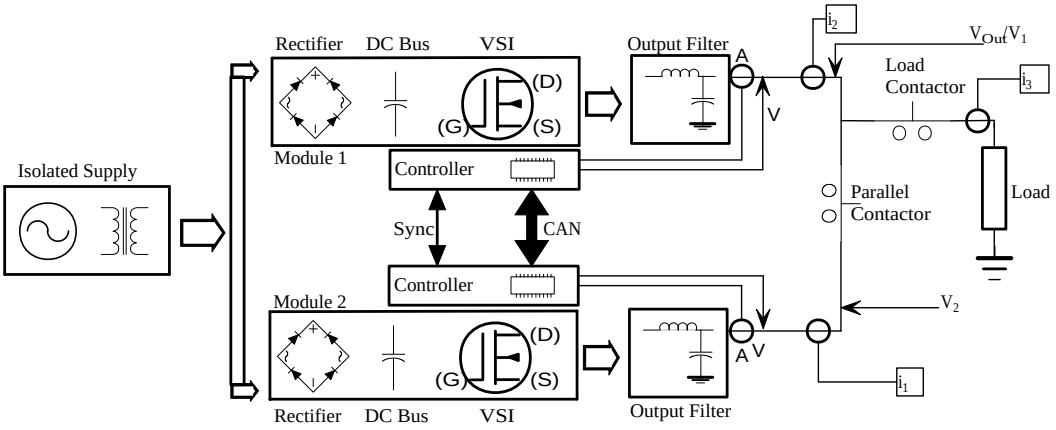


Figure 6.1 Parallel Module Test Setup

6.2.2 Layout

A schematic of the test setup is shown in fig 6.1. Fig 6.2 is a photograph of the actual test setup including the two modules with controllers, the output filters, and the contactors. Fig 6.3 shows a close up of the controllers on top of their respective power modules, showing the communication lines and common mode output chokes. Fig 6.4 shows the independent output sensing elements for current and voltage for each module. The only links between modules except for the common supply and output buss are the two communication lines.

6.2.3 Measurement Points

Measurement points i_1 and i_2 measure the current being sourced from module 1 and module 2 respectively. Circulating current is found by taking $i_1 - i_2$. The current probe at i_3 measures the total output current of the system. v_1 measures the system output voltage. All scope traces are taken from a TEK THS720 scope using the Wavestar software application. Current measurements are made using a Fluke 80i 1000s AC current probe, and voltage measurements taken using a Yokogawa 700924 differential isolated voltage probe, except in the case of measurements made with the Fluke 41 meter which are measured directly.

Circulating current is the most observable indicator of load imbalance. For the most part it is the variable that will be tracked to indicate quality of load sharing. With only two modules the circulating current can be measured directly with a single probe. This provides a much more accurate indication of what is occuring than inspecting the current waveforms of each module. The method of direct measurement is shown in figure 6.5.

6.2.4 Common Mode Path

During the design phase the potential for significant zero sequence current flow between modules was acknowledged. The anticipated cause was the asynchronous switching of paralleled modules due to the absence of a synchronisation routine operating at the switching frequency. The reason it was not addressed in the single phase prototype is that the intended output filter had significant common mode inductance, so the resulting common mode current flow would be insignificant. Synchronisation would become vital in the case of a three phase system using a 3 limb choke. Cost effectiveness often demands 3 limb output chokes are used for 3 phase systems, and as these have very low common mode inductance common mode current flow would be large with the expected common mode voltages.

The oversight in design was that since the output filter inductor was only present on one of

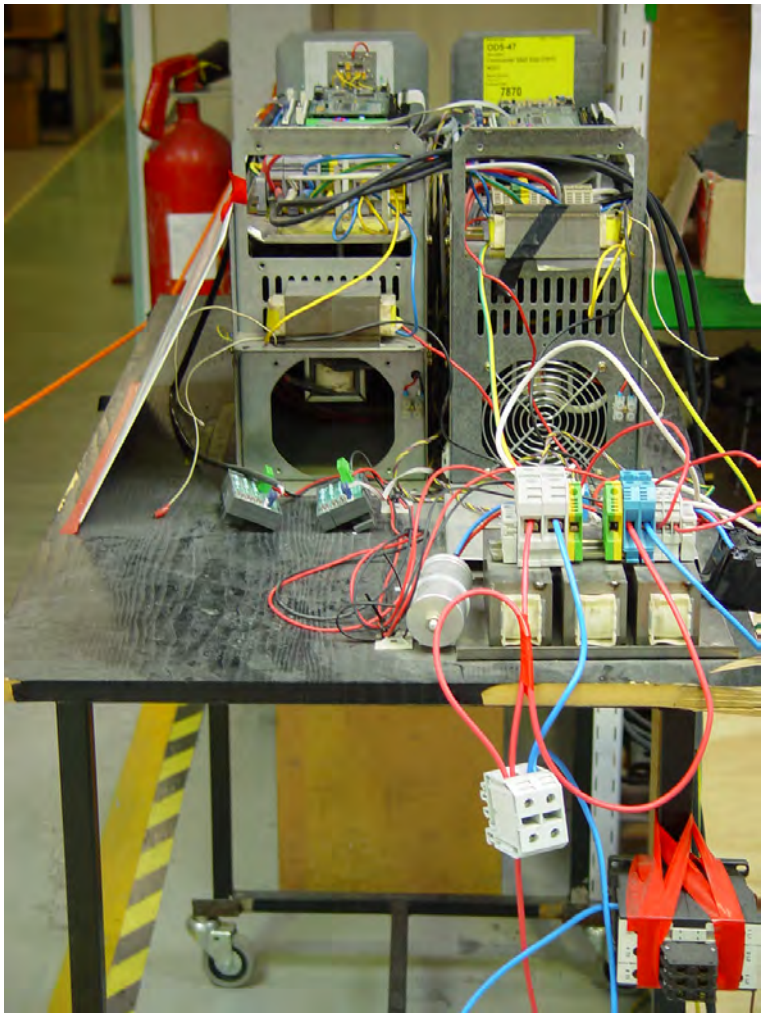


Figure 6.2 Complete system including output filters and contactors

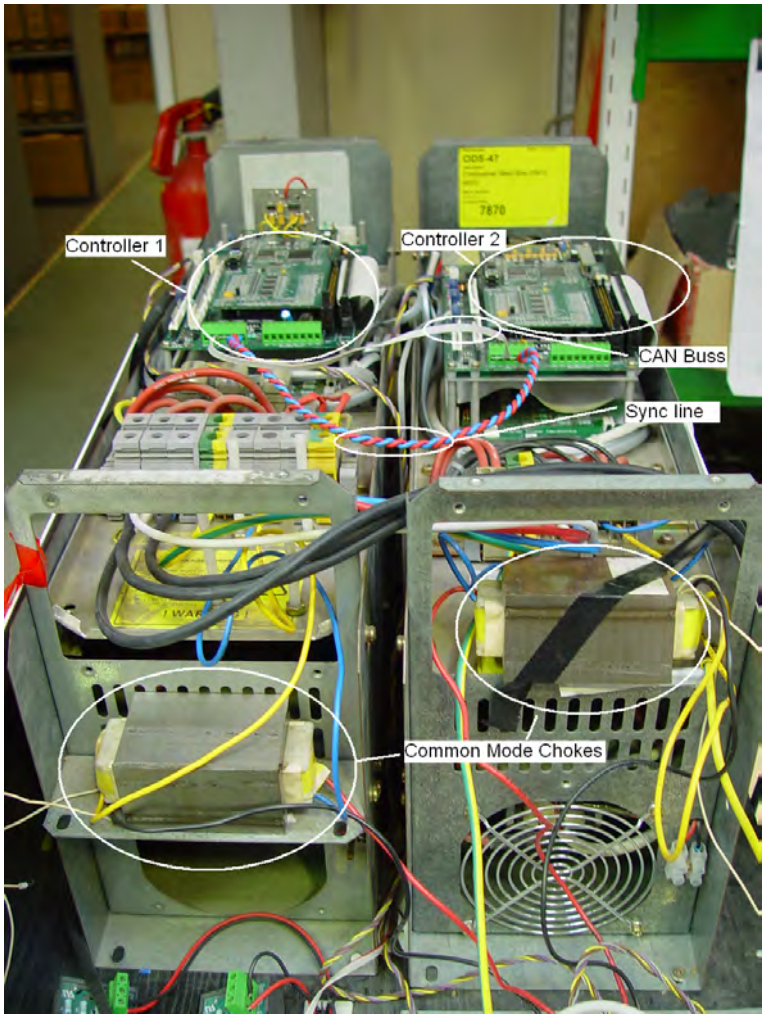


Figure 6.3 Power and Control Stage

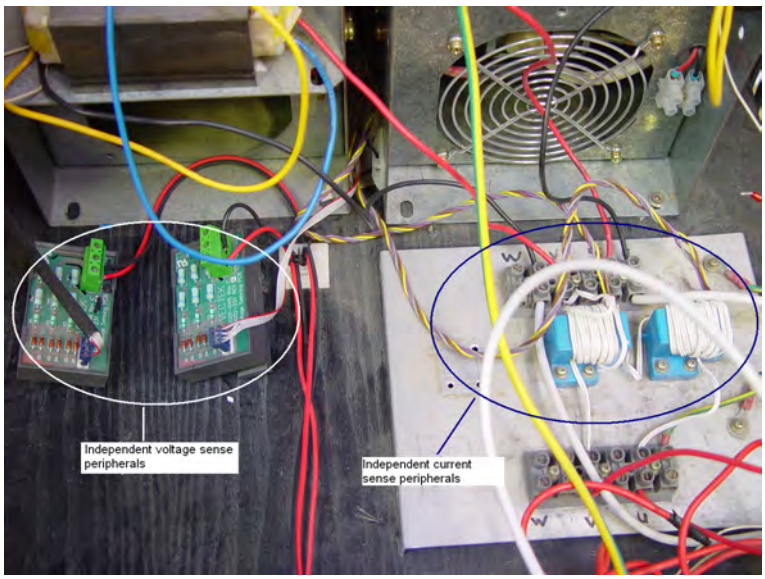


Figure 6.4 Sensing Peripherals

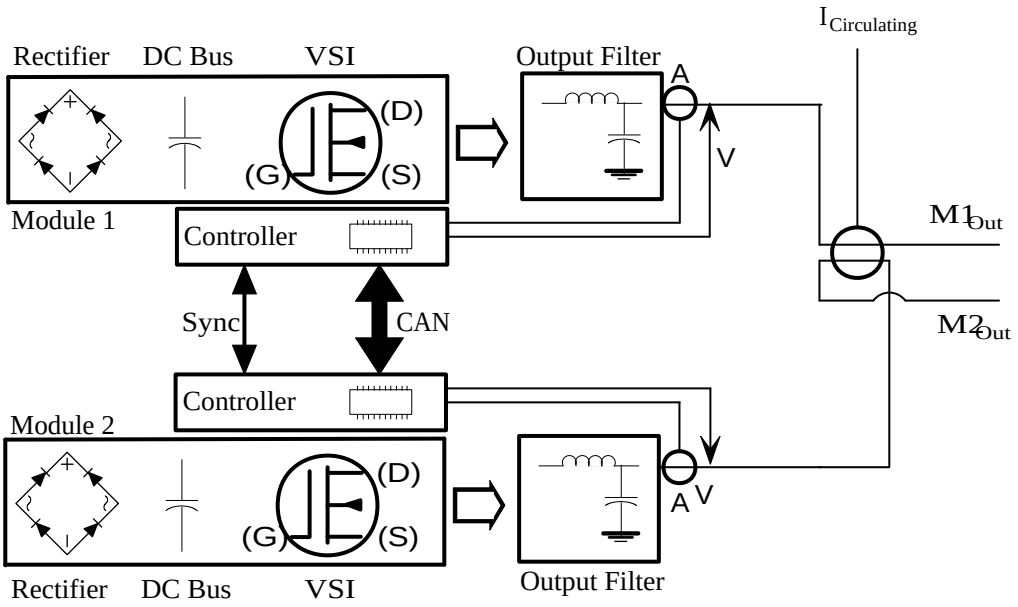


Figure 6.5 Method of Measurement of Circulating Current

the two output lines a common mode path with near zero inductance still existed, as shown in figure 6.6. Initial tests without the common mode chokes exhibited huge common mode current flow. Common mode chokes were added to the output of each module, as shown in Fig 6.3. It must be emphasized that the inclusion of common mode chokes in the module outputs is not a preferred long term solution. An improved synchronisation routine to provide synchronous or near synchronous switching will need to be implemented before this system is suitable for commercial use.

6.3 TEST PROCESS

The primary objective of this research was to find a method by which multiple VSI modules in parallel could share load with a high level of precision and stability. The ideal would be a system in which all modules had identical instantaneous currents at all times, and the difference between the output voltage and the reference voltage was no greater than the difference between those two voltages in a single module system with the same load conditions. Achieving this ideal outcome is unrealistic, but the aim is to come close; tolerances have already been set out.

Frequency domain analysis is used as this allows clear illustration of the effects of increasing delay, and the results from such a technique are easily linked to limitations such as control loop bandwidth. To illustrate the nature of imbalance identified by inspection of the circulating current, the current waveforms of each module will be simultaneously recorded for comparison.

Testing is conducted for communication delay intervals across and beyond the range of stable operation using both slow and fast local droop control algorithms. The areas investigated are:

- Current sharing between paralleled modules with a linear load.
- Current sharing between paralleled modules with a non-linear load.
- Current sharing between paralleled modules during a step load transition.
- Voltage distortion at the output of the paralleled modules running into a linear load.

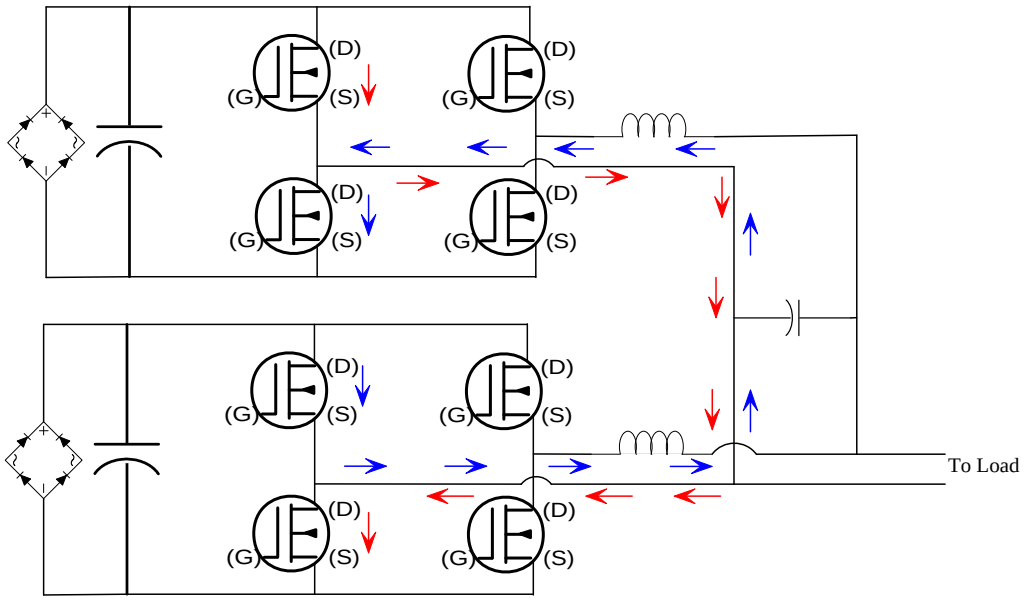


Figure 6.6 Common Mode Current Path

6.4 LINEAR LOAD CURRENT SHARING

The load used for this phase of testing is $2.4kW$ at $230V$ drawing unity power factor. Test setup is as described above. Key points of interest are:

1. The imbalance of current between the two paralleled modules, measured as a percentage of the nominal module output current.

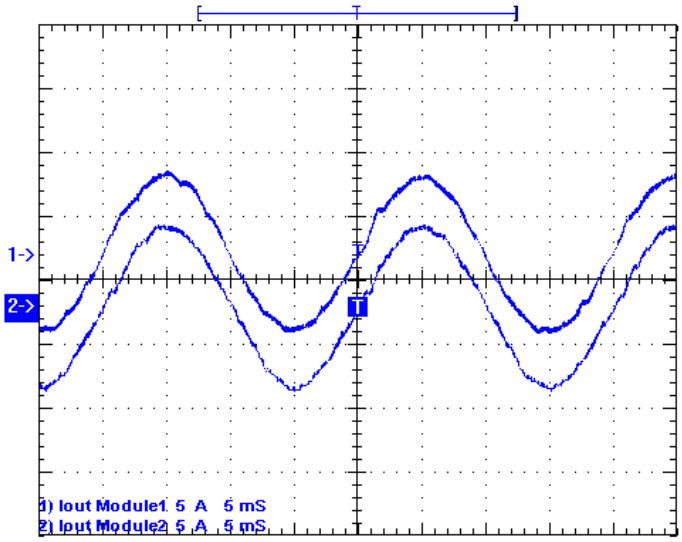
2. The stability of the local module control loops, and hence complete system.

6.4.1 Slow Local Voltage Droop

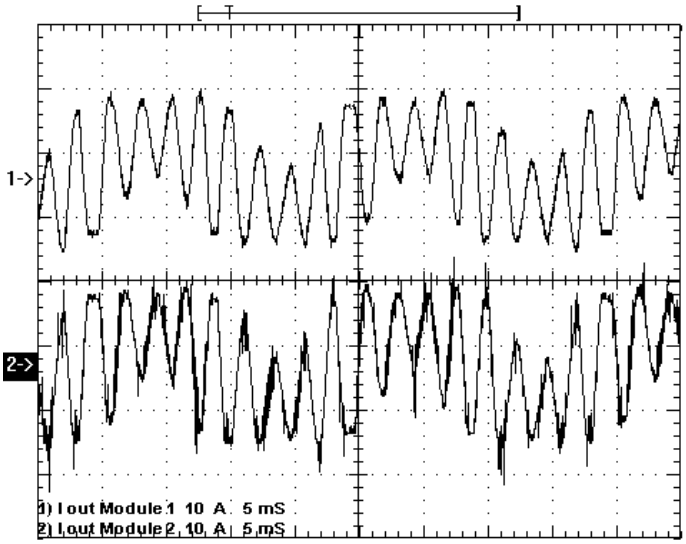
This algorithm was designed to avoid the output voltage error present in the fast local droop system due to an effective non-differential output impedance. With slow local droop, the droop term feeding back into the control loop is updated at the same rate as the global average current term, a zero order hold term in the feedback loop providing the delay. All other local control has access to the usual high update rate local current.

The trend of increasing circulating current to the point of instability is immediately apparent from these results. Using a synthetic resistor value of $0.2p.u.$, the system becomes unstable with an introduced communications delay of $7t_s$, but gives good load sharing at $3t_s$. The module current waveforms shown in figure 6.7(a) show the balanced waveforms acheived with small communications delay ($delay = 3t_s$), while figure 6.7(b) clearly shows the instability exhibited with a larger communications delay ($delay = 7t_s$).

This can also be clearly observed by inspection of the circulating current between modules, measured as described in the system setup. Waveform captures at the small and larger communication delays of $delay = 3t_s$ and $delay = 7t_s$ are shown in figure 6.8. The contrast is clear, circulating current in the $3t_s$ case is minimal and at frequency outside the range of the control loop, and is primarily due to the asynchronous switching of the modules. In the $7t_s$ case however it represents the majority of module currents, which would exceed the system rating and lead to excessive device stress and module trip/failure were this system truly running at its rated load.

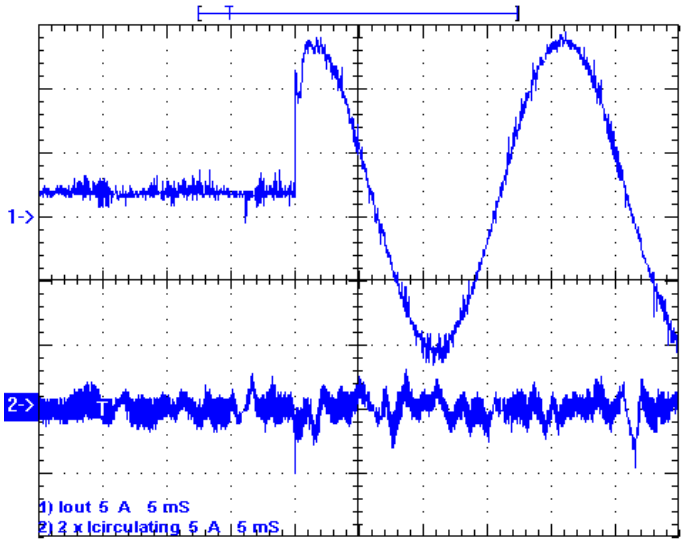


(a) Delay = $3t_s$.

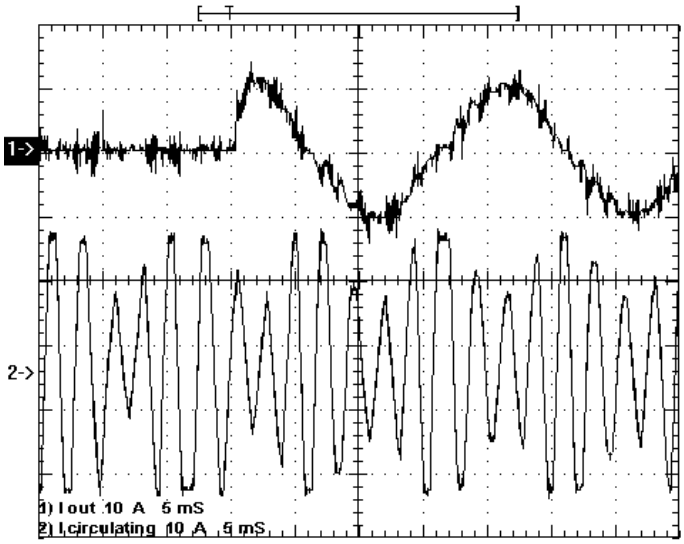


(b) Delay = $7t_s$.

Figure 6.7 Comparison of module currents under Slow Local Droop - Linear Load



(a) Delay = $3t_s$.



(b) Delay = $7t_s$.

Figure 6.8 Comparison of system output current with intermodule circulating current under Slow Local Droop - Linear Load

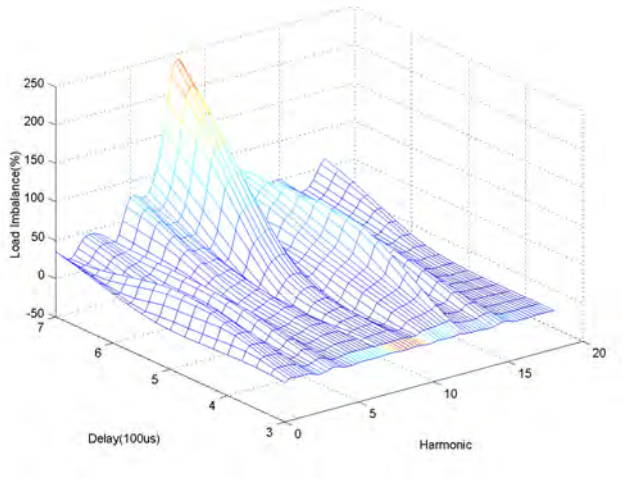


Figure 6.9 Circulating current harmonics at varying communication delays under Slow Local Droop - Linear Load

Figure 6.9 shows the effect of the increasing communications delay over a wider range of values, clearly illustrating the previously discussed importance of high bandwidth communications frameworks to allow high rate sharing. This system will not meet the design requirements for current sharing if the communications delay exceeds the minimum shown value of $3t_s$, but delivers good performance at that delay.

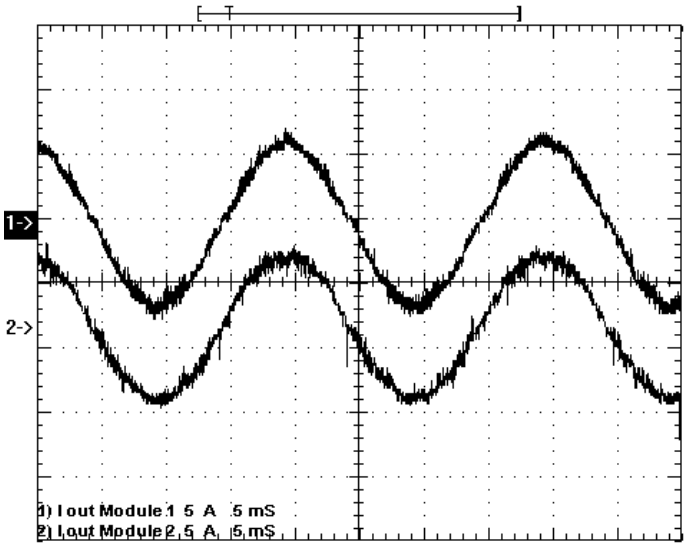
6.4.2 Fast Local Voltage Droop

With the fast local droop response the system remains stable at significantly larger communication delays, as shown by the individual module output currents in fig 6.10. The low intermodule circulating current, even at large delays, is clearly illustrated in fig 6.11. However, Fast Local Droop has a significant cost, as discussed during simulation, in that it is essentially a hybrid droop/differential droop system. The effect of this hybrid nature will be apparent in the later section on quality of response, suffice to say that while the circulating current is low at delays that are easily realisable for systems with large numbers of modules, it's operation at these large delays does not provide satisfactory performance and should not be viewed as an option.

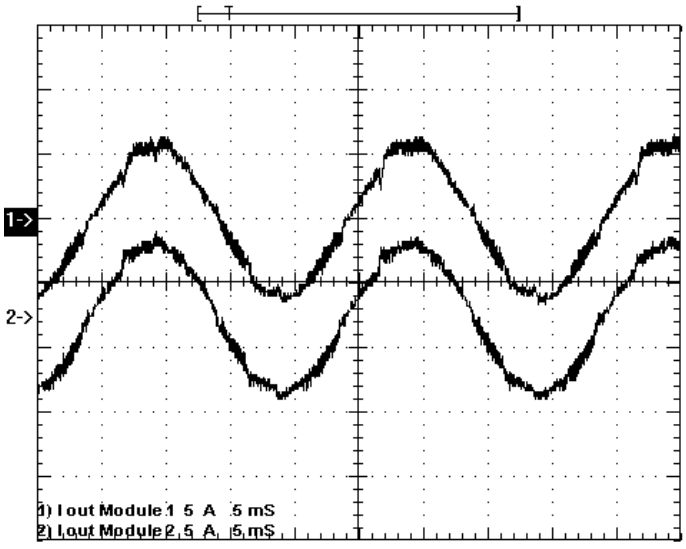
Figure 6.12 shows the effect of the increasing communications delay over a wider range of values under the fast local droop scheme. As expected from the theory, the current imbalance does not become excessive even at very high delays. This is because under fast local droop the local impedance term is always present; the global term simply compensates for its distortion of the output at intervals of whatever the communications delay happens to be. This result cannot be considered in isolation, as theory tells us to expect unacceptable output voltage distortion at high delays when using fast local droop, but certainly the load balancing is well within requirements.

6.5 NON-LINEAR LOAD CURRENT SHARING

This test was conducted by placing a rectifier and capacitor between the CCP and load. If the algorithm is capable of balancing harmonic currents as well as the fundamental it will significantly increases the utility of the system, as many commonly encountered loads draw large harmonic currents.

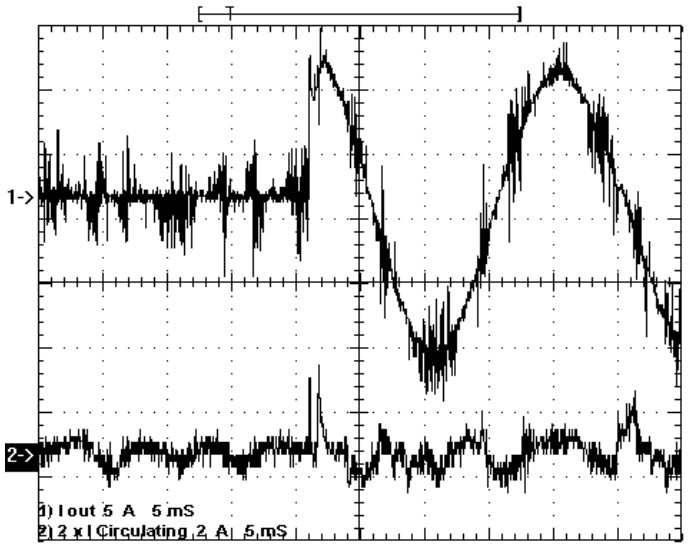


(a) Delay = $7t_s$.

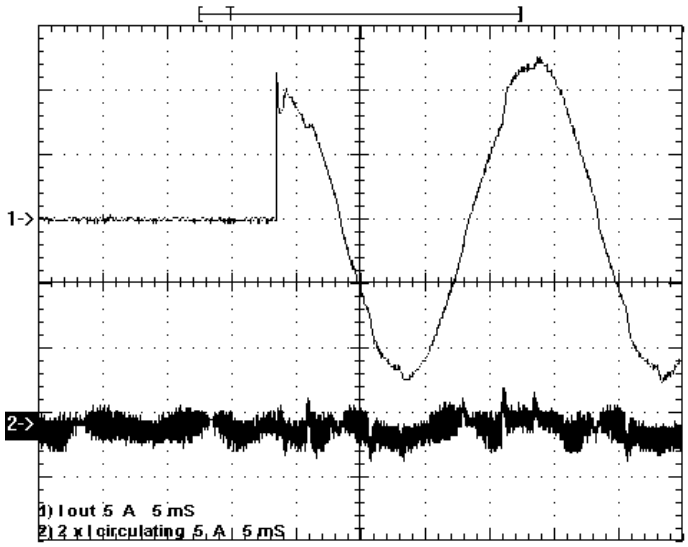


(b) Delay = $15t_s$.

Figure 6.10 Comparison of module currents under Fast Local Droop - Linear Load



(a) Delay = $7t_s$.



(b) Delay = $15t_s$.

Figure 6.11 Comparison of system output current with intermodule circulating current under Fast Local Droop - Linear Load

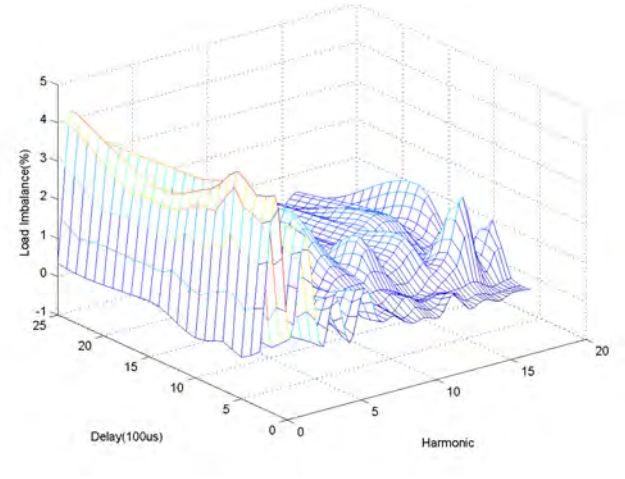


Figure 6.12 Circulating current harmonics at varying communication delays under Fast Local Droop - Linear Load

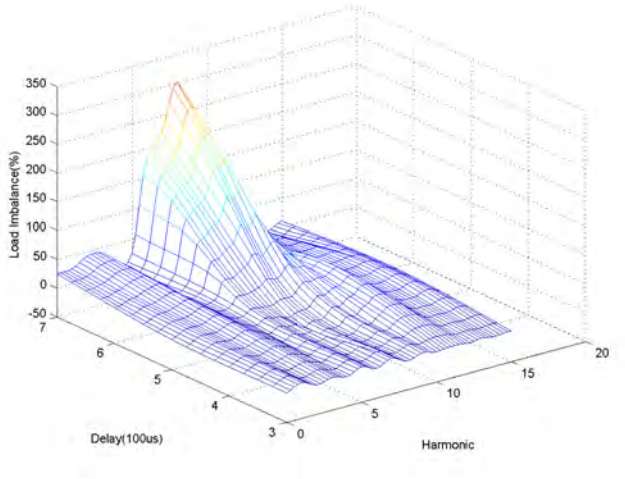


Figure 6.13 Circulating current harmonics at varying communication delays under Slow Local Droop - Non-Linear Load

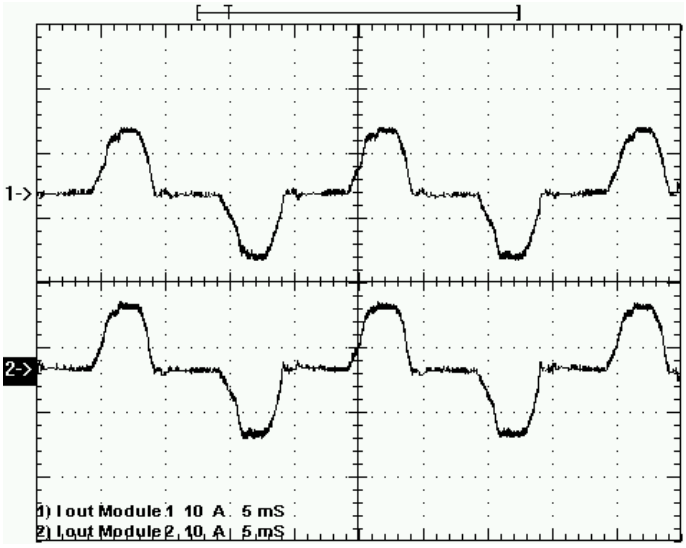
6.5.1 Slow Local Droop

Waveform captures are not presented for the slow local droop non-linear load case as they are functionally the same as for the linear load case. The current is balanced well for the $3t_s$ case and the system is unstable from $7t_s$. This is clearly illustrated in the harmonic analysis shown in fig 6.13.

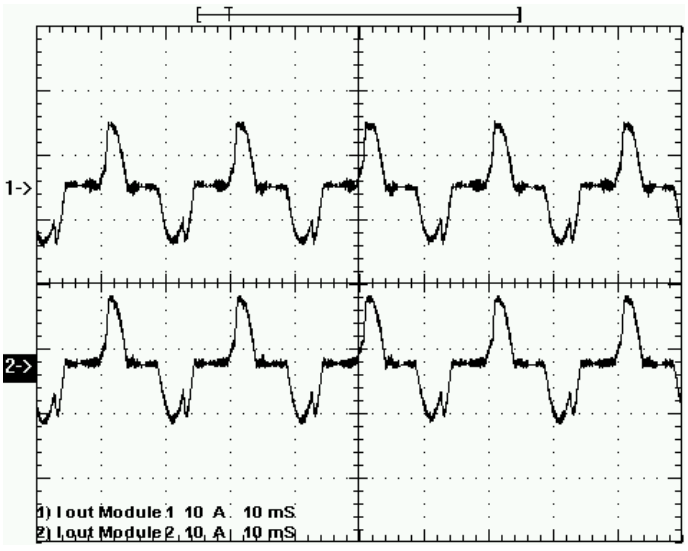
6.5.2 Fast Local Droop

The waveform captures of the module currents in the fast local droop case are of interest due to the prominence of the effect of the change in effective output impedance at the moment the global current is updated in the high delay case. This is very apparent when comparing the two cases in 6.14.

The circulating current in the non-linear load case under fast local droop control is once again well constrained, but as discussed in the linear load case this is only acceptable if the voltage



(a) Delay = $7t_s$.



(b) Delay = $25t_s$.

Figure 6.14 Comparison of module output currents at varying delays under fast local droop - Non Linear load

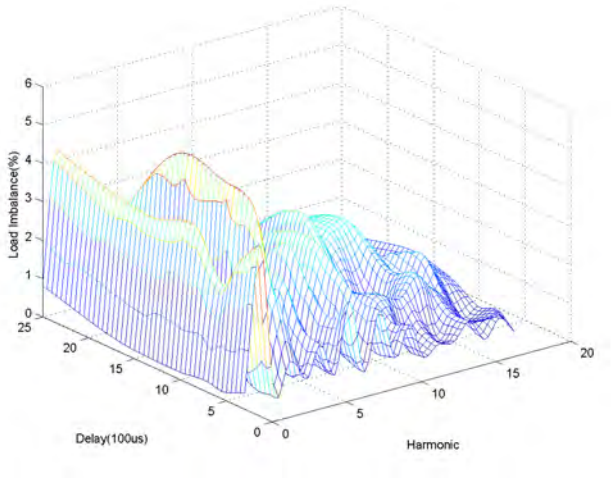


Figure 6.15 Circulating current harmonics at varying communication delays under Fast Local Droop - Non-Linear Load

distortion is also sufficiently small. The circulating current at the full range of communication delays is shown in fig 6.15.

6.6 STEP LOAD TRANSITION CURRENT SHARING

The step load test was conducted by running the system in parallel with the load contactor open, and then closing it with the linear load described for the previous test attached. The results show the parallel systems response to a load transient. This is relatively unimportant in a system with a small number of modules, as even fairly high momentary imbalances will likely be tolerated by the abused module, however substantial imbalances in large systems will easily destroy an over-exerted device, or at the very least cause protection to operate. Good current balance during the step load change demonstrates the differential droop algorithms ability to balance transient load as well as steady state load. Also of significant interest is the systems absolute stability under transient conditions, as differential droop with delay is of little use if it balances current at the expense of system stability.

6.6.1 Slow Local Droop

The $delay = 3t_s$ case only is given as the $delay = 7t_s$ will never be stable under a transient if it was unstable in steady state. Inspection of the results shows good stability at the high data rate, as shown in fig 6.16. Circulating current is minimal as is output current distortion. There is no evidence of ringing or marginal stability at frequencies within the system bandwidth.

6.6.2 Fast Local Droop

Once again the results for two different rates are given for the fast local droop case. The delay $= 7t_s$ case in fig 6.17 demonstrates the good output current control and well balanced response of the system under a readily achievable operating condition. The delay $= 25t_s$ case in fig 6.18 clearly illustrates the action of the non-differential impedance term, the output current (and hence voltage) collapsing slightly before being corrected. While both responses are completely stable and share load adequately, only the low delay response will be suitable for the final system, as the large delay result represents too great a distortion of the voltage.

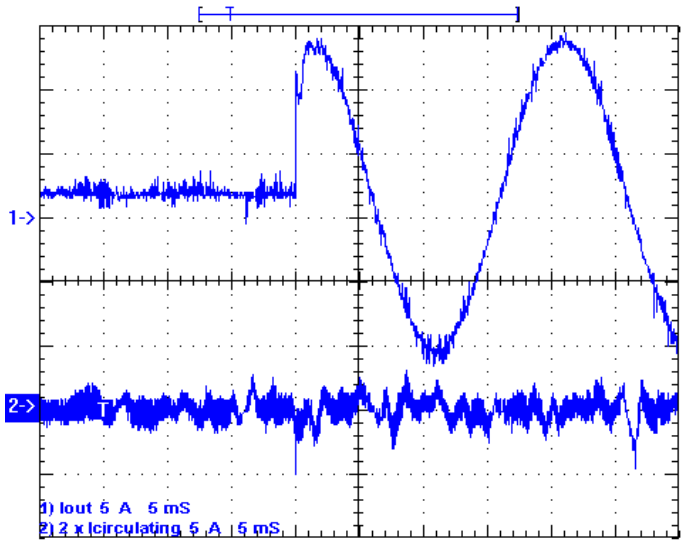


Figure 6.16 Output and intermodule circulating current under step load transition at delay = $3t_s$ under slow local droop control

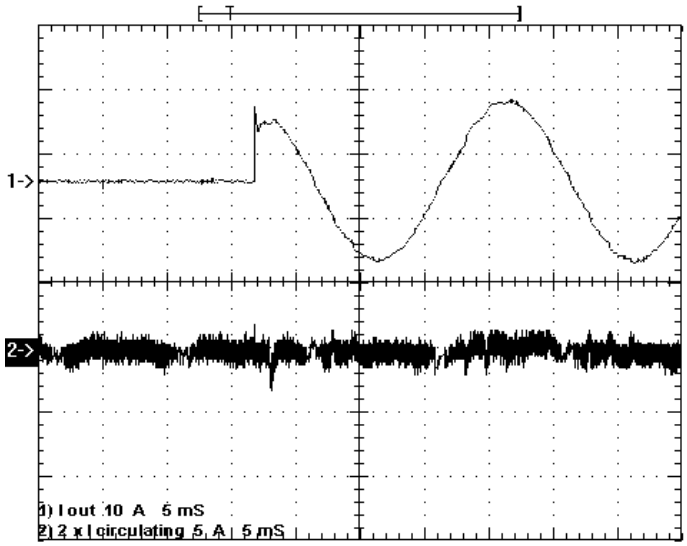


Figure 6.17 Output and intermodule circulating current under step load transition at delay = $7t_s$ under fast local droop control

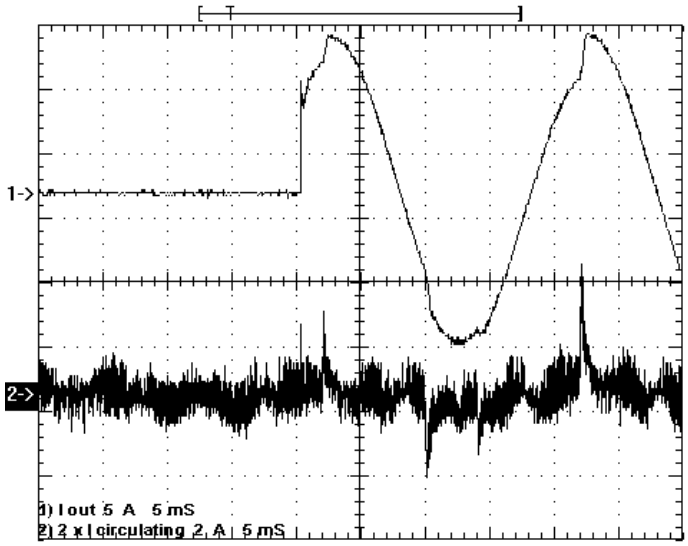


Figure 6.18 Output and intermodule circulating current under step load transition at delay = $7t_s$ under fast local droop control

6.7 LINEAR LOAD VOLTAGE DISTORTION

Parallel operation is a valueless attribute if it comes at a high cost to the quality of the systems output. The initial application of the parallel technology is expected to be power quality units. These units are intended to compensate for deviations from nominal supply voltages, so if they themselves introduce a deviation through the action of the parallel load sharing loop then they are essentially useless. This section investigates the fidelity of the system with regard to the reference input. Our specification requires an output voltage distortion of less than $\pm 1\%$ compared to nominal voltage.

6.7.1 Slow Local Droop

Figure 6.19 shows the voltage error at relevant harmonics for the slow local droop control loop. Distortion is near zero in the identified stable operating region, an exceptionally good result. The huge error at higher delays is no surprise, nor any additional inconvenience as it was unstable at those points anyway. Based on this result it is reasonable to conclude that slow local droop, supported by the control structures developed and implemented in the previous chapter, is an appropriate control method for paralleled VSI modules providing the communications delay is not greater than $3t_s$.

6.7.2 Fast Local Droop

Figure 6.20 shows the voltage error with the high rate local droop control loop. The constraints on the operating region of the previously high performing fast local droop algorithm now become apparent. While it remains stable at low delays and continues to balance intermodule circulating current effectively, the output voltage distortion at communication delays greater than $5t_s$ are greater than the limits laid out for this design. This is consistent with the theory, and as discussed in chapter 4 there are methods that can be used to correct the distortions, but the ideal would be to run the network at a sufficiently low delay so as to avoid an error in the first place.

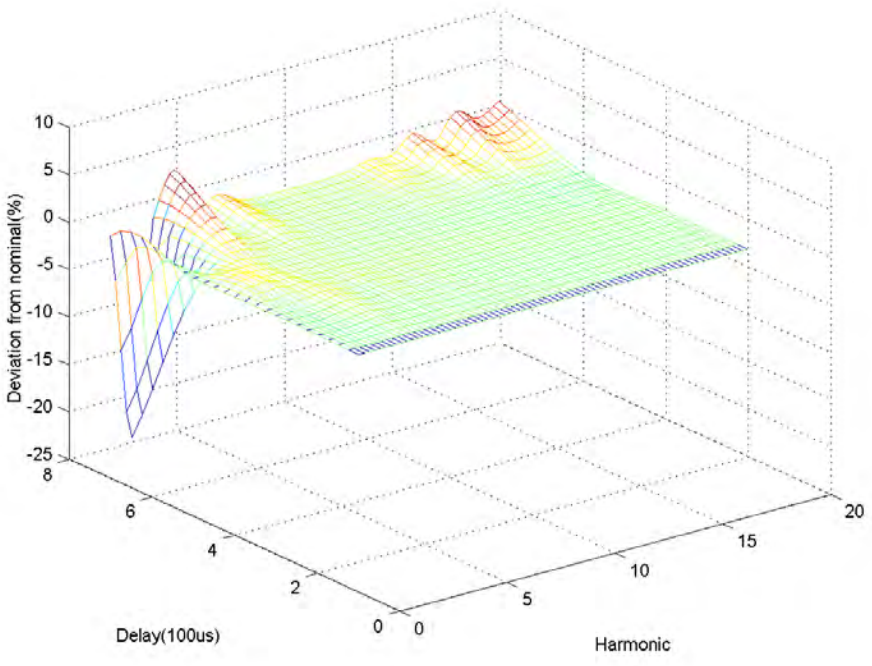


Figure 6.19 Voltage deviation from nominal using slow local droop sharing

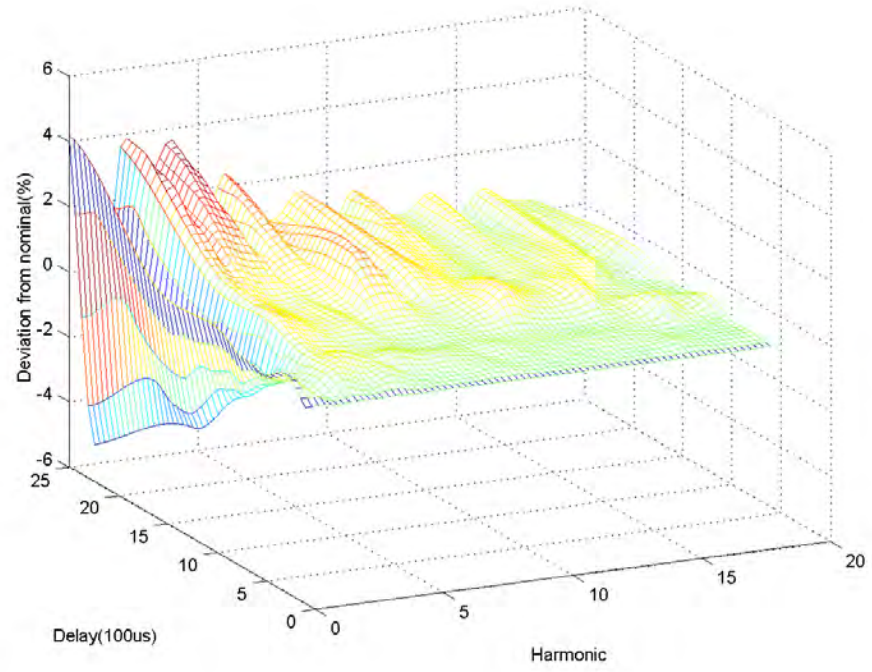
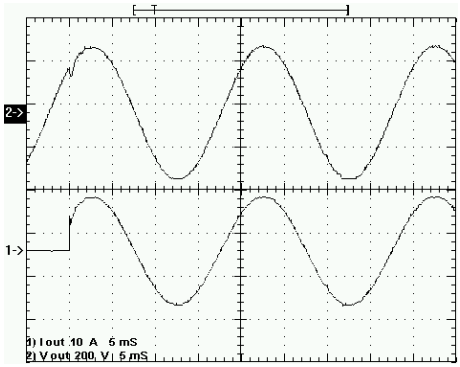
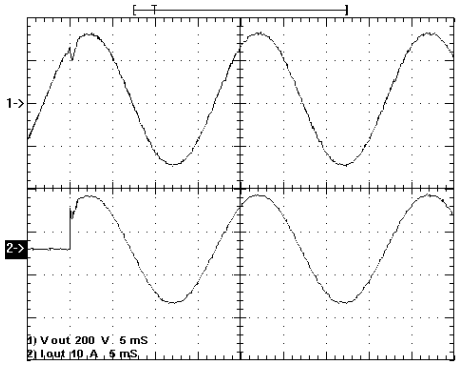


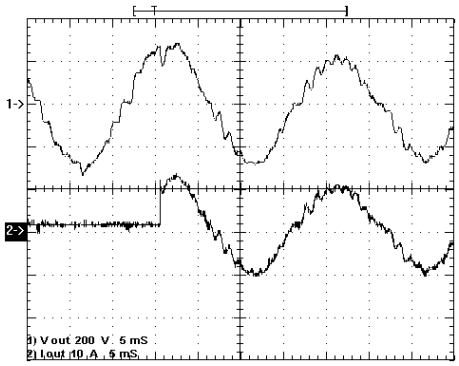
Figure 6.20 Voltage deviation from nominal using fast local droop sharing



(a) Interval = 3.



(b) Interval = 5.



(c) Interval = 7.

Figure 6.21 Step load response of paralleled units under slow local droop control.

6.8 STEP LOAD TRANSITION TRANSIENT VOLTAGE DISTORTION

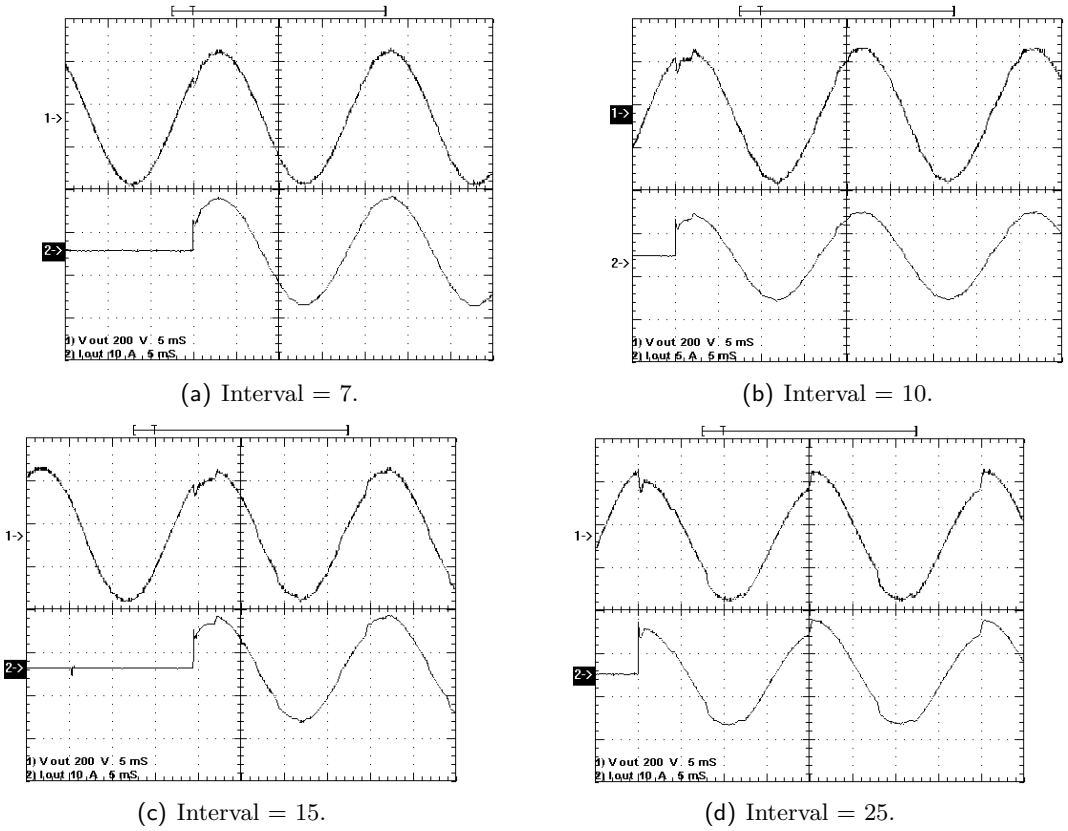
As in the load sharing analysis, the step load response cannot easily be expressed in terms of harmonic makeup. The short term distortion can be observed however, and in the case of unstable sharing mechanisms the distortion is readily apparent.

6.8.1 Slow Local Droop

The slow local droop results are given in fig 6.21. As is by now fairly expected, the slow local droop algorithm delivers good results at a delay of $3t_s$, and also gives a more than adequate result at $5t_s$. Beyond this point however the output is heavily distorted and clearly unstable. The underlying voltage control algorithm however performs adequately at the delay rates previously identified as suitable, and is not disrupted by a step load transition.

6.8.2 Fast Local Droop

The fast local droop results are given in fig 6.22. Once again, the fast local droop algorithm delivers a clearly stable result at all delays, but progressively increase output distortion as delay increases. The response for the delay = $7t_s$ is completely stable and delivers acceptable transient distortion, however the harmonic voltage analysis put the delay limit for fast local droop at delay = $5t_s$ to conform to the steady state distortion requirements. By inference the result at this delay rate would be more than acceptable.



(a) Interval = 7.

(b) Interval = 10.

(c) Interval = 15.

(d) Interval = 25.

Figure 6.22 Step load response of paralleled units under fast local droop control.

6.9 AGREEMENT WITH SIMULATION?

The low bandwidth algorithms mentioned in chapter 4 and presented briefly in Appendix B have not been implemented in software or tested on the available hardware due to a shift in the intended development path, as outlined in chapter 7, making such testing redundant. However, the simulation results can still be validated to a certain extent by inference. The only variation between the different load sharing methods both in simulation and real world implementation is the method by which the differential droop term is calculated and the rate at which it is updated. A change in method should have the same effect in the real world as it did in simulation, the uncertainty is whether the Simulink model is an accurate representation of the real world system. To determine this, the experimental results of this chapter and the results of the simulation are juxtaposed. A close similarity between the two under similar simulated conditions gives credibility to the simulink model and in doing so qualifies the results of the low bandwidth sharing mechanism simulations made using the model.

6.10 SUMMARY

The system developed to allow stable and high performance active paralleling of VSI modules has been fully tested for its effect on the output voltage and the accuracy with which load balancing can be achieved. The results agree with the theoretical expectations, the performance requirements of the specification have been achieved within the system constraints by either the fast or slow local droop control methods. However, the sensitivity of the method to the inter-module communications delay has been conclusively demonstrated, and is a significant weakness of the method. The topologies requirement for steadily increasing bandwith proportional to the

number of modules in the system places a real limit on the maximum achievable system size. Lessons learnt in the development of the algorithm have given inspiration for an alternative improved control topology that will not face this limitation, a brief introduction to which is presented in chapter 7.

Generally however, the experimental results are extremely gratifying and conclusively prove the suitability of differential droop combined with waveform synchronisation as a method to balance load between paralleled VSI modules with a high degree of accuracy without distorting the systems output voltage.

Chapter 7

REVISED CONTROL ARCHITECTURE AND PERFORMANCE ANALYSIS

7.1 INTRODUCTION

The previous chapter demonstrated the performance of a multiple master system operating in parallel using a differential droop mechanism. While effective, the method used had significant drawbacks, key among which was the limited number of modules able to be included for a given intermodule communication bandwidth constraint. This chapter identifies limitations of the solution as tested in the previous chapter and describes an alternative control architecture and differential droop algorithm developed to overcome the limitations. The performance is simulated to give empirical evidence of its benefits.

7.2 LIMITATIONS OF MULTIPLE MASTER CONTROL

The key problem with the multiple master approach used to calculate the global current in the tested incarnation of the parallel control algorithm is that it requires each controller on the network to globally broadcast its current. Each module added to the system places additional load on the communications channel as indicated in figure 7.1. The plot is for a sharing rate of $500\mu s$ and does not allow for additional channel bandwidth required for routine communications such as fault handling, variable updates etc. If the load sharing were able to be achieved through a single master/multiple slave hierarchy, then only one broadcast per sharing interval would be required regardless of the number of modules operating on the system, dramatically reducing the bandwidth requirement.

7.3 ALTERNATE ARCHITECTURE DEVELOPMENT

The key strengths of the initial mechanism were good stability and performance at low loop delays. The key limitation was the difficulty of maintaining these low delays with a large system. The performance and stability were due to the efficacy of the differential droop algorithm, so an alternate implementation was developed that retained differential droop based sharing, but altered the control architecture and system structure to reduce the communication requirement.

7.3.1 Proposal

The load sharing control loop shall use the master modules locally measured current level as a substitute for the global current value previously calculated by averaging all the modules local currents. This will reduce the bandwidth requirement as only one variable will need to be shared

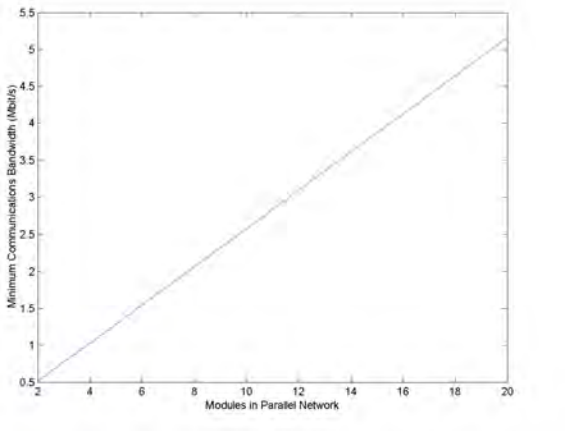


Figure 7.1 Bandwidth requirement under multiple master control with increasing network size

in each delay period. Obviously this de-correlates the communication load from the number of modules in the system, allowing much greater system sizing for a given bandwidth.

7.3.2 Complications

Structural changes to the controller were required to support the new topology. The following are the difficulties encountered in the transition and the means by which they were overcome.

Control Asymmetry

The primary concern with transition from multiple master to master slave structure is that the introduction of an asymmetric element to the control loop will have an adverse effect on system stability, requiring revisions to the control algorithm. Initial simulation results were unsuccessful, becoming unstable with even small communication delays and droop coefficients. Inspection revealed the control loop asymmetry to be the cause. Effectively the master module was operating with no droop term at all ($i_{local} - i_{local} = 0$), and the slave modules attempting to droop relatively to maintain a balanced load. While theoretically stable in a zero delay environment, the single sample time communication delay was enough to destabilize the system. To correct this, rather than having different control transfer functions for the master module and slave modules the slave algorithm was used on all modules, and the master structure redesigned to piggyback on the nominated master module rather than being an integral part of the control loop. In this piggyback mode, the locally held droop variables update at the same rate as the globally held variables, thus restoring symmetry to the system. This adds a slight delay to the loop, but nothing more than was encountered in the best of the multiple master systems, and with a lower bandwidth requirement.

System Management

The second complication of the transition to a master-slave system is that some method of master module reassignment must be developed and implemented to allow continued (though slightly derated) operation of the parallel network if the existing master module suffers a failure. Basically this reassignment algorithm must result in the same functionality as the multiple master network offered, the key points being

1. Detection of module failure by inference: The slave modules should be able to recognise a fault on the master module without the master module necessarily broadcasting a fault

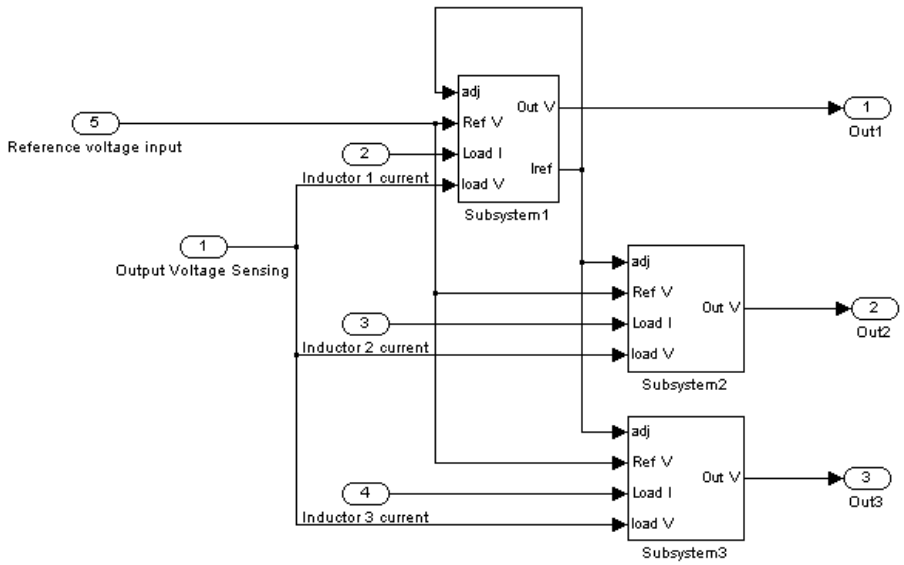


Figure 7.2 Control Flow Diagram for Symmetrical Master-Slave system

message. The simplest mechanism would be to interpret a failure to provide a scheduled reference variable as a fault.

2. Clean transfer: The failure and reassignment process should not result in significant output distortion (significant being distortion of concern to the load).

3. Multiple failure tolerant: The system should be tolerant to the successive failure of several master modules and allow reassignment of the controlling module until it is reduced to a single unit system.

4. Modularity: Ideally the software structure should allow additional modules to be integrated into the network without having to change the software on the existing modules.

7.4 CONTROL ALGORITHM MODIFICATION

The modification to the control loop is very simple as all the key internal structures remain unchanged, the only difference is that modules no longer need to publish their local current, and no longer need to perform any collation and averaging action. Instead, the global current through the common output buss is measured by the master, normalised to a value appropriate to the number of modules in the system, and published to all modules simultaneously. Using a RS454 dataline this can be accomplished within a single control loop iteration, greatly improving the transient response of the system. Modules then droop their local reference according to the difference between the nominal average instantaneous current and their local current.

7.5 SIMULATION RESULTS

The results given are matlab simulations of the systems performance. External factors are identical to those previously simulated with the multiple-master system.

Figure 7.3 shows the results for the system operating under conditions the same as those of the initial simulations in chapter 4. Sharing is stable and voltage distortion is minimal, proving that the revised algorithm does not sacrifice the previously demonstrated benefits of the master-master differential droop algorithm. Figure 7.4 shows the same test conducted with reference

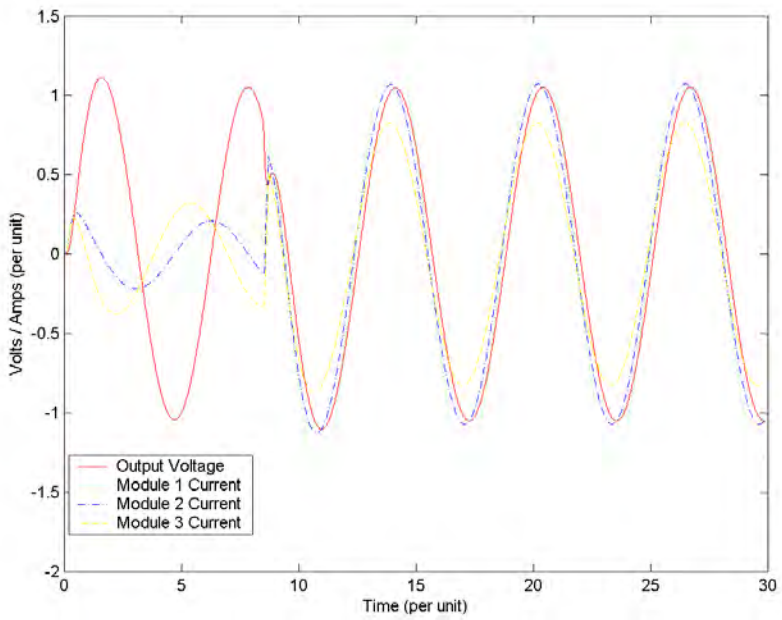


Figure 7.3 Simulated Voltage and Currents for Revised Master-Slave Differential Droop Compensated System

distortions of ±1% rather than the ±5% distortion used until now. This gives a more accurate idea of the load balancing that can be expected with the waveform generation accuracy proven easily achievable with the reference waveform synchronisation techniques used

Load imbalance and voltage distortion for this case are presented in figure 7.5.

The change in presentation of results is due to the beauty of this system in that there is never a need to increase the intermodule communication delay due to the one-to-many topology. Where previously a steady degradation in performance was observed as the sacrifices necessary to accommodate a large system were made, namely increased sharing delay, the new topology allows the best case communications delay regardless of the number of modules in the system. The system performance is exceptional in all cases.

7.6 SUMMARY

A comparison of simulation results between the oringinal system and the modified system topology and control algorithm strongly favour the modified system. Performance achievable with low numbers of modules is comparable, but with the large systems which this research aims to facilitate the performance increase with the modified control method is huge. If a robust communications framework is available then the modified control topology and algorithm should be able to support very large systems within the constraints of an readily achievable datarate.

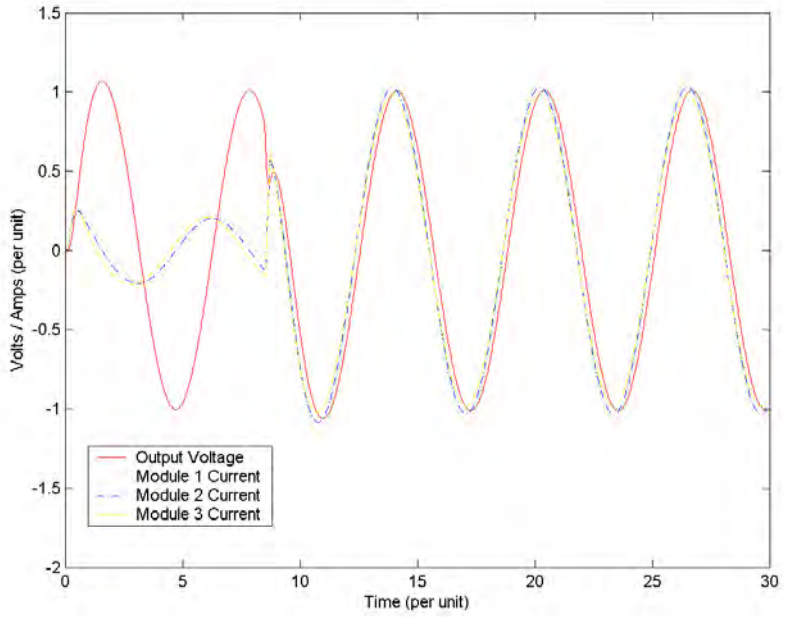
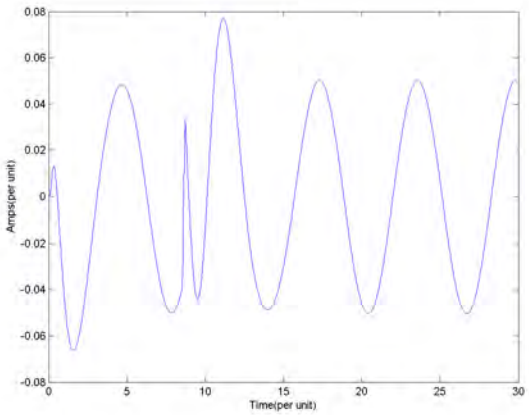
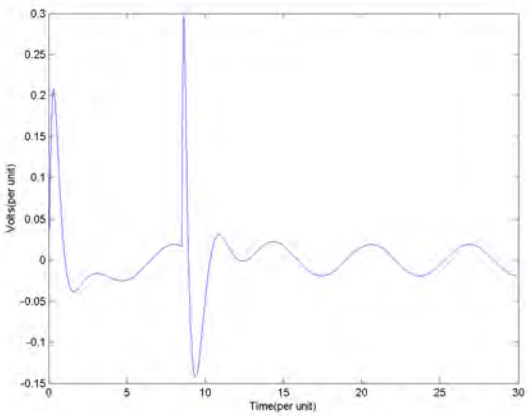


Figure 7.4 Simulated Voltage and Currents for Revised Master-Slave Differential Droop Compensated System with low reference error



(a) Module Load Imbalance



(b) Output Voltage Distortion

Figure 7.5 Load Imbalance and Voltage Distortion for low error case at standard delay

Chapter 8

FURTHER DEVELOPMENT

8.1 INTRODUCTION

This chapter suggests a path for continued development of the system. The first two items are additions to the system deemed necessary to allow a transition from promising prototype to commercially viable product. The remainder are possibilities identified during development and deemed worthy of further research, but not investigated sufficiently to report on in the main body of work.

8.2 CARRIER WAVEFORM SYNCHRONISATION

As discussed in the report on test results, common mode voltage differences between modules is a significant issue in these systems. The majority of the common mode results from small differences in the carrier frequencies and/or phase alignment of the PWM carrier waveforms. Synchronising the carrier waveforms between modules would mean that only the difference in reference waveforms caused common mode voltage differentials. This would result in a huge reduction in common mode circulating current and noise. The sync line between modules could be readily utilised to facilitate this carrier synchronisation. Invariably the controllers will be active before the output is enabled, which allows time to align carriers.

8.3 PARAMETER MANAGEMENT

The highly distributed nature of the control method used in the proposed system combined with the high dependence on symmetry of control response requires that a reliable parameter management scheme operates within the system. The current proposal is to allow the master to exercise additional supervisory control, and the slaves to derive all control parameters from the master on startup. The anticipated mechanism is the CAN framework, with checking and updating of control parameters performed during the system boot process.

8.4 ONLINE CALIBRATION AND OPTIMISATION

One area of control theory that is not applied in the parallel loop is that of self-optimization. The probable source of the majority of the voltage error term has been identified as discrepancies in feedback elements, primarily voltage but also (to a lesser extent) current sensing. If it is assumed that these discrepancies are the sole cause of the error, and they are assumed to be constant, then the feedback elements can be modified to zero the discrepancies and hence zero (or at least reduce) the error producing term.

This technique is limited however by the requirement to assume that the sensed values are accurate to within the tolerances that the system is to be optimised to. Without an accurate feedback element, optimisation cannot occur.

8.5 COMPARTMENTALIZATION OF LARGE NETWORKS

While it has not been investigated in this research, and indeed is not an issue on a purely theoretical basis, there is likely to become a point at which a large systems spatial separation means equal-footing paralleling of modules is no longer the most practical option. There are a variety of possible issues, including environmental factors, communications network limitations, and segregation of systems for redundant fault response. The differential droop principle can be layered, with local masters under the control of a global master for example, but the implications of this action, or alternatives, at varying data rates needs to be investigated before extremely large systems can be considered feasible.

8.6 PARTIAL FAILURE

The premise of this research is that the goal of a parallel system control mechanism is the equal sharing of load between all modules within a system. In an ideal world this would be the case, however situations could exist in which the optimum load distribution was asymmetric. An example of this would be partially obstructed airflow on a single module leading to reduced effective load capacity. Considering the usual system response would be to at best isolate the faulty module, and probably trip the entire system, reducing the load on compromised modules until they are able to be serviced increases the average accessible system capacity, which increases the value delivered. The control framework allows for arbitrary load distributions, and the benefits of doing so should be investigated with the goal of adding value to the system.

8.7 CONTROL GENERALISATION

This research was conducted with the aim of developing a parallel VSI control architecture for a power electronics companies product range. The success of this project has given confidence that development of a medium power module able to be paralleled as required to provide the necessary rating is both possible and beneficial. A module based on this paralleling principle and intended for application to a voltage conditioning product range is now in the final stages of development. The control method is intended to be implemented on marine shore power systems in the near future, and eventually paralleled power modules are expected to be the basis of all the companies VSI products operating above a medium power level of about 100kW.
The work required to facilitate this transition is still significant. The developments mentioned earlier in this chapter will form the basis of the system, and are as yet not implemented in software. The paralleling scheme itself will be able to be implemented without a lot of modification from the existing scheme. The majority of the software work will be in development of the rotating master hierarchy and fully redundant fault handling system.

8.8 SUMMARY

The developed technology is very promising and has delivered sound results thus far, but further refinements are required prior to its commercial application. No major obstacles are anticipated to its commercial use. Further to the initial commercial application there is significant scope for further research and development, with particular emphasis on increased achievable availability

and capacity factors. Increased transient response is a secondary area of interest in the initial applications, as the existing transient response is already satisfactory, however if the technology is applied to more demanding environments then opportunities for enhancement exist within the developed topology and control structure.

Chapter 9

CONCLUSION

Semiconductor based power electronics form the basis of most modern low to medium electrical power conversion technology, and there is every indication that their utilization will continue to grow. A particularly large opportunity for expansion is in high power applications, where the potential for improvements in performance offered by high bandwidth active systems are huge. Presently however, as identified in this research, the limitations to the practical operating envelope of existing devices and topologies in terms of power and transient response are a significant obstacle to their use in high power systems (>1MW).

This thesis aimed to dramatically increase the achievable operating envelope through developing a method by which multiple power semiconductors could operate in parallel with minimum reduction in capacity and controllability. This would allow near arbitrarily large systems to be implemented that were able to extract full benefit from the high bandwidth control options already developed for low power systems.

A review of existing techniques for paralleling of power semiconductors revealed a number of areas for improvement. While some techniques have been developed that allow stable paralleling, no existing technique combined the identified system requirements of reliability, maintainability, fast transient response, high fidelity, and efficiency.

A new control method and associated system topology were developed. The system structure envisages modular system components, each with an independent local controller linked to other modules by two robust 1Mbit rate differentially driven omnidirectional communications links. Following performance analysis and refinement of the control technique to incorporate a centralised master controller these were supplemented with a 4Mbit unidirectional one-to-many line.

The control method developed is termed differential droop. It involves the comparison of load variables local to a modular element with a system average of the same variables. The output reference is adjusted to correct imbalances based on the difference between the local value and system average. The key difference between this control method and widely used linear droop based load sharing is the output reference adjustment inserted in a differential droop scheme sums to zero across the system. This causes no reduction in output fidelity, unlike linear droop schemes which distort the system output as the load varies. Extensive simulation and proof of concept testing indicated the developed control method would be effective in achieving them requirements of the specification.

Software was developed to implement the differential droop algorithm, including mechanisms to synchronise reference waveforms and system parameters. The control method was tested on a small representative parallel system of two single phase inverters each re-scaled to operate at 1.2kVA nominal load. Output fidelity was essentially unchanged from a single module system, and load sharing was within the design specification for both steady state and transient operating conditions. Once calibrated, steady state voltage distortion at full load under the optimum

control method was less than 0.5% of nominal; and load imbalance was less than 2% of nominal. These tolerances are more than adequate for the system anticipated, the voltage distortion is well within the specification of ±1%, and the load imbalance requires minimal over-rating of the system. Furthermore, a major limiting factor in these accuracies is the ADC on the DSP controlling the modules. Transition to a higher resolution DSP would further improve performance, as would the online adaptive tuning algorithm discussed in Chapter 8. The underlying differential droop algorithm has the potential to deliver near ideal results. The primary limitation is the ratio of $\frac{di}{dt}$ to t_{delay}. Mathematically, the output distortion reduces to zero if the sharing delay is low enough, and communications frameworks are available which allow this to be achieved at power system fundamental frequencies.

To summarise, a new control algorithm and system topology have been developed to allow multiple inverter modules with local control and management to perform as one large module without sacrificing reliability or performance, and without the need for significant overrating. The algorithm balances load between modules on a steady state and transient basis without distortion of the system output. The algorithm has been tested on a small power prototype and delivered results substantially superior to the hard connection topology currently employed. A commercial product has been developed based on the improved algorithm and proposed system topology, and has been released as a replacement for an existing system operating using hard paralleling technology. Performance meets or exceeds the replaced products performance in all regards, and the maintainability, cost, reliability and mean time to repair have all been vastly improved. The algorithm and topology are a major step forward and are seen as an enabler for a range of technologies penetration into new markets.

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Appendix A

POWER FLOW BETWEEN ACTIVE SOURCES

Load sharing in generation grids is accomplished by drooping the frequency in response to increased power flow. Increased power flow demands an increased electromagnetic torque on the rotor of the generator. If the electromagnetic torque is greater than the mechanical torque, the rotor will decelerate. This has the effect of reducing the power angle between the rotor and stator, which reduces the electromagnetic torque, hence equilibrium is rapidly restored, albeit with a drop in frequency. This drop in frequency propagates through the grid, and increases the power angle at other generators, resulting in their deceleration, leading to an overall drop in frequency with the increase in power requirement. The frequency is determined by the angular velocity, which also determines the voltage. Hence an additional feedback element is obviously required to avoid a sustained voltage error whenever the load moves away from nominal. This response is a change in mechanical input power proportional to the change in speed. By this method, all generators on a grid will (assuming identical per unit droops) self regulate such that they are all producing the same per unit power.

With an inverter the load equalisation action is not inherent to the system. Equalising loads between modules, while not necessarily based on droop characteristics, is a matter of ensuring that the power angle and voltage amplitude of an inverters output with respect to the common bus is proportional to that inverters rating and output impedance. Modules with equal rating and output impedance should have equal phase and amplitude. A module with lower impedance would have smaller phase difference and amplitude. A module with a higher rating would have a larger phase difference and amplitude and so on.

The problem posed by parallel VSI's is similar to that of a generation grid. Multiple units, most capable of bi-directional power flow, are required to each transfer a specified amount of power in a given direction. The main difference is that in a generation grid the per unit power transferred by different units may vary significantly due to differing costs of generation from different sources, while the units in the parallel system will typically be operating at a common per unit load.

With the accurate control of power flow as our goal, it is sensible to begin with an understanding of the key factors affecting power flow. When considering a parallel array of inverters all sharing a common output bus, the power handled by a given inverter is dependent on not only its own output conditions, but also by the conditions at the common bus, which are in turn affected by all the other units connected to that bus. Therefore we need an expression linking power flow through an inverter with the conditions at the inverters output and Common Connection Point (CCP).

Figure A.1 shows an inverter (modelled as a voltage source) connected to a quasi-active grid. Clearly by controlling the power flow between (1) and (2) we are controlling the power flow through the inverter.

In an AC system with the above parameters, real power (P) flows between (1) and (2) according

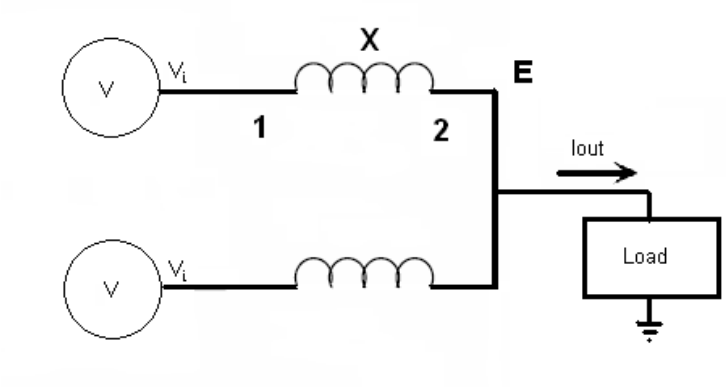

Figure A.1 Power Flow Between Active Sources

to

$$P = \frac{V_i E sin\phi}{X} \tag{A.1}$$

and reactive power (Q) flow is given by

$$Q = \frac{V_i E cos\phi - E^2}{X} \tag{A.2}$$

where X is the impedance of the line, V_i is the rms equivalent voltage at the output of the inverter, E is the rms voltage at the CCP, and ϕ is the power angle, or the angle by which the voltage at (1) leads the voltage at (2).

From inspection of the two above equations, we can see that at low power angles, the real power P depends primarily on ϕ, while the reactive power Q depends primarily on the difference in amplitude between V_i and E.

Both V_i and ϕ are easily set by the inverter, so we have our means of controlling power flow, with P and Q able to be varied largely independently of each other. Our controllers ability to select and assert some instantaneous voltage at the point (1) will be the determining factor in the success of the system. Selecting different values of V_i and ϕ for different modules will determine how much power each module carries. The sensing topology used in the voltage/current control loop described in Appendix C allows direct measurement of the voltage amplitude and phase at point (2).

Appendix B

BANDWIDTH EFFICIENT PARAMETER SHARING

Early in the development of the differential droop algorithm it became apparent that the system was heavily dependent on a low inter-module communications delay to achieve maximum performance with regard to output voltage fidelity. Bandwidth being a scarce resource on the platform at the time, the following schemes were developed and considered as a low-rate alternative to simple sample-and-hold sharing.

B.1 PULSE TRANSMISSION TO SINEWAVE INTERPOLATING FILTER

This system samples the local current at a rate just about the nyquist rate for the fundamental waveform. This is distributed among all modules. The average value is found, scaled to account for the effects of decimation, and filtered to extract the fundamental element.

The advantage of this system is that the rate of communication can be substantially reduced without a negative impact on the sharing accuracy while retaining good steady state voltage regulation. The current sharing, shown by simulation in figure B.1, is as good as for any of the other fast local droop schemes. However, as shown in the simulations results of figure B.2, the transient performance of the system with regard to voltage distortion is terrible. The system eventually recovers as the filter output shifts to match the new load, but the output voltage error for the filter time constants simulated is unacceptable.

This system is also inadequate in that it will only provide a differential droop response for loads drawing current at the fundamental only. Any harmonic current will cause a harmonic voltage error on the output. This system is unsuitable as the sole means of provision of a differential droop action as its response is far too slow.

Figure B.4 and B.3 show the performance of the pulse interpolation sharing mechanism at a number of pulse transmission rates in the same format as the results presented in chapter 4.

B.2 AMPLITUDE AND PHASE SHARING NETWORK

This is essentially a variation on the above allowing even lower rate communications. By calculation and sharing of the local current phase and amplitude, modules could reconstruct the average current waveform using a very slow comms net. No relative phase information will be contained in the load sharing signal, so this method requires a synchronisation line between modules, however synchronous reference waveforms and PWM carriers have already been shown to be vital so this synchronisation requirement is not an overhead.

This system retains all the weaknesses of the above system with regard to transient response and harmonic distortion, and is hence likewise unsuitable given the requirements of the system under development.

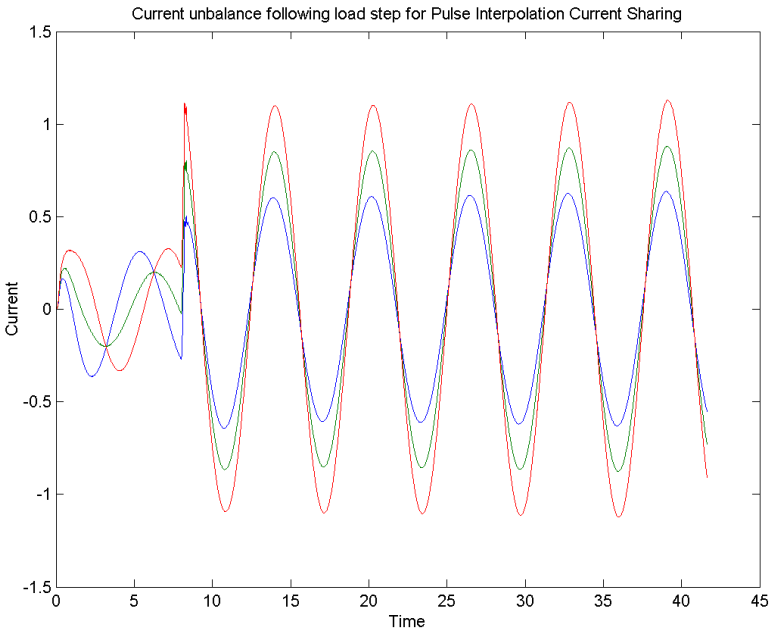

Figure B.1 Module Currents for Pulse Interpolation Based Sharing

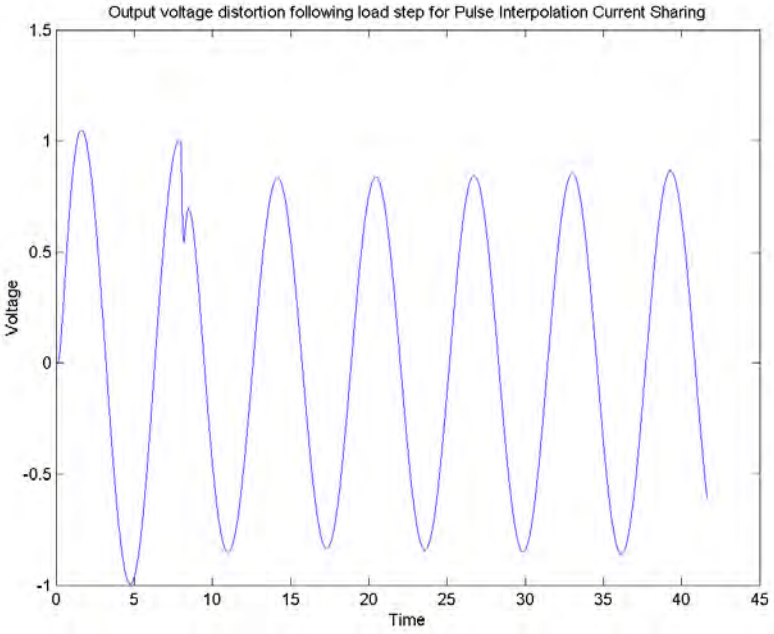

Figure B.2 Output Voltage Distortion for Pulse Interpolation Based Sharing

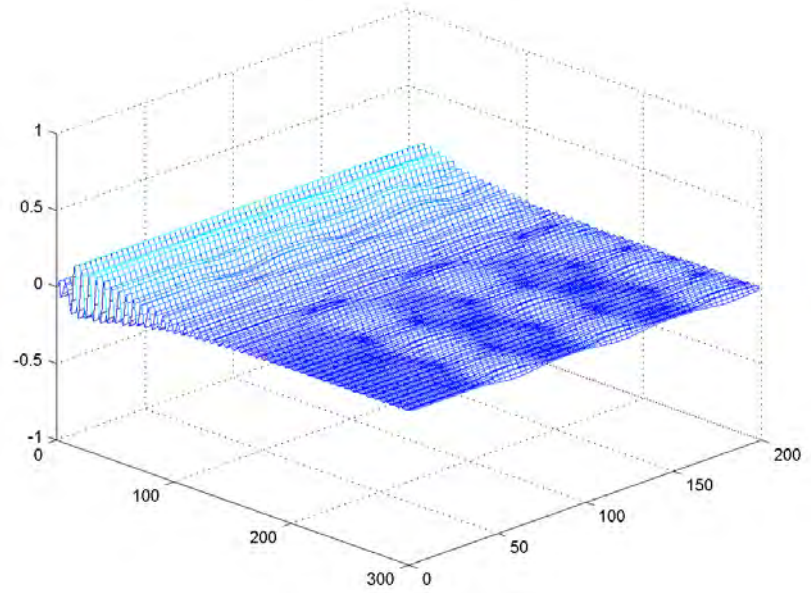

Figure B.3 Output Voltage Distortion at Varying Communication Delays

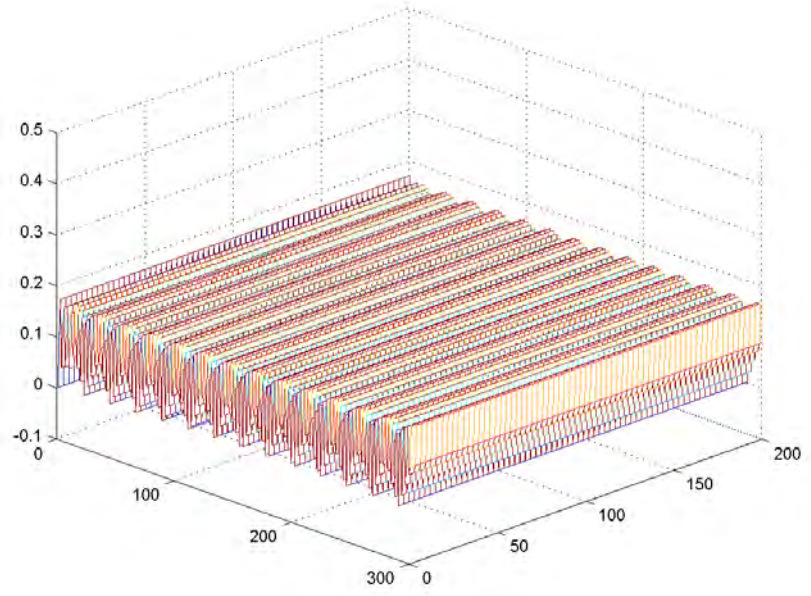

Figure B.4 Module Load Imbalance at Varying Communication Delays

B.3 ADAPTIVE MULTIRATE SYSTEM - HYSTERETIC CONTROL

The inspiration for this system came from the realisation that the majority of the time the system was in a fairly stable mode of operation and either of the above mechanisms would provide adequate performance while allowing free bandwidth for the CAN to be used for system housekeeping in addition to load sharing. The high bandwidth mechanism is only really necessary in the event of a load transient. The multirate system therefore operates the low rate amplitude and phase network the majority of the time. However, if the following identity becomes true

$$|V_{out} - V_{ref}| > threshold$$

then it is assumed that some event has occured to make the slow routine inadequate, and the system immediately transitions to the fast zero order hold mechanism. Operation continues using the fast mechanism until the voltage error drops below the threshold and remains below for a period sufficient to allow the slow routine to adapt.

This system provided performance equal to that of the system developed in chapter 4 with a significantly lower average bandwidth requirement. It was not implemented in the initial design/test phase due to its increased complexity, and was then superseded with the development of the revised control scheme with the dedicated SDI communications network. It would be worthy of consideration in other systems that could support momentary high data rates, but required the communications network for other functions as well.

Appendix C

LOCAL CONTROL LOOP

This thesis has treated the voltage controller running on each module as something of a black box, as its function is slightly irrelevant to the theory of the differential droop action. However, it does have implications on the systems stability and transient response, and so is presented briefly here in the interests of completeness. In the early stages of development a deadbeat controller optimised for the target system was considered and developed to a simulation level, however the performance improvements that demonstrated in simulation were insufficient to justify the time required to transition across to the new controller, so it was abandoned.

The controller used in the experimental systems and all simulations is shown in fig C.1. It operates a closed loop on both the voltage and current - the inductor current and the capacitor voltage specifically.

The capacitor current is decoupled from the output inductor and output voltage variations, and controlled directly to set the output voltage. A particular distinguishing feature of this system is the use of a resonator instead of an integrator. This gives zero gain at DC, avoiding problems with overamplification of a DC error, while retaining an integrative error compensation response at the fundamental frequency of the system. This controller gives good transient response and zero error under steady state conditions, but tends to require re-tuning of the control parameters, in particular the resonator gain, for some loads. This was the main attraction of a shift to the deadbeat controller, which was designed to self tune. The developed differential droop algorithm should be tolerant of a shift in voltage control algorithm, and such a shift could offer moderate performance improvements - hence should be reconsidered at a later date if more time becomes available.

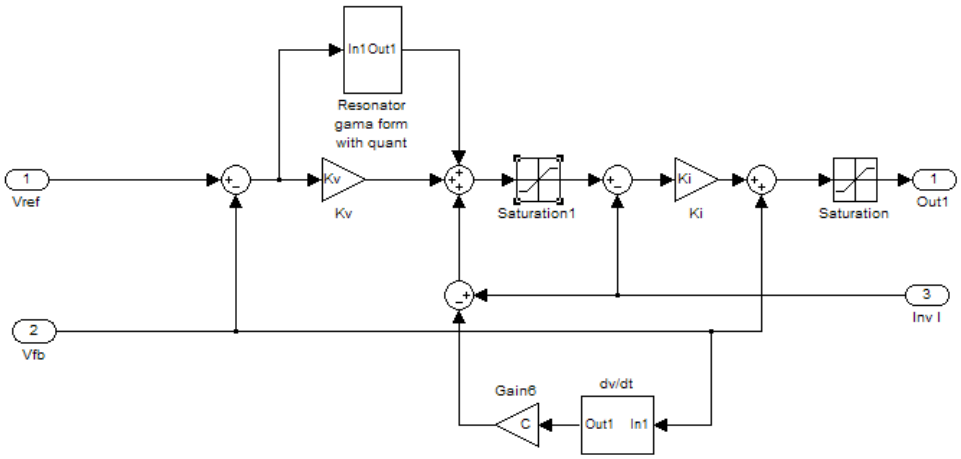

Figure C.1 Local Control Loop: Closed loop Voltage and Current control